ANALOG ELECTRONIC CIRCUITS
LAB MANUAL

III SEMESTER B.E (E & C)

(For private circulation only)

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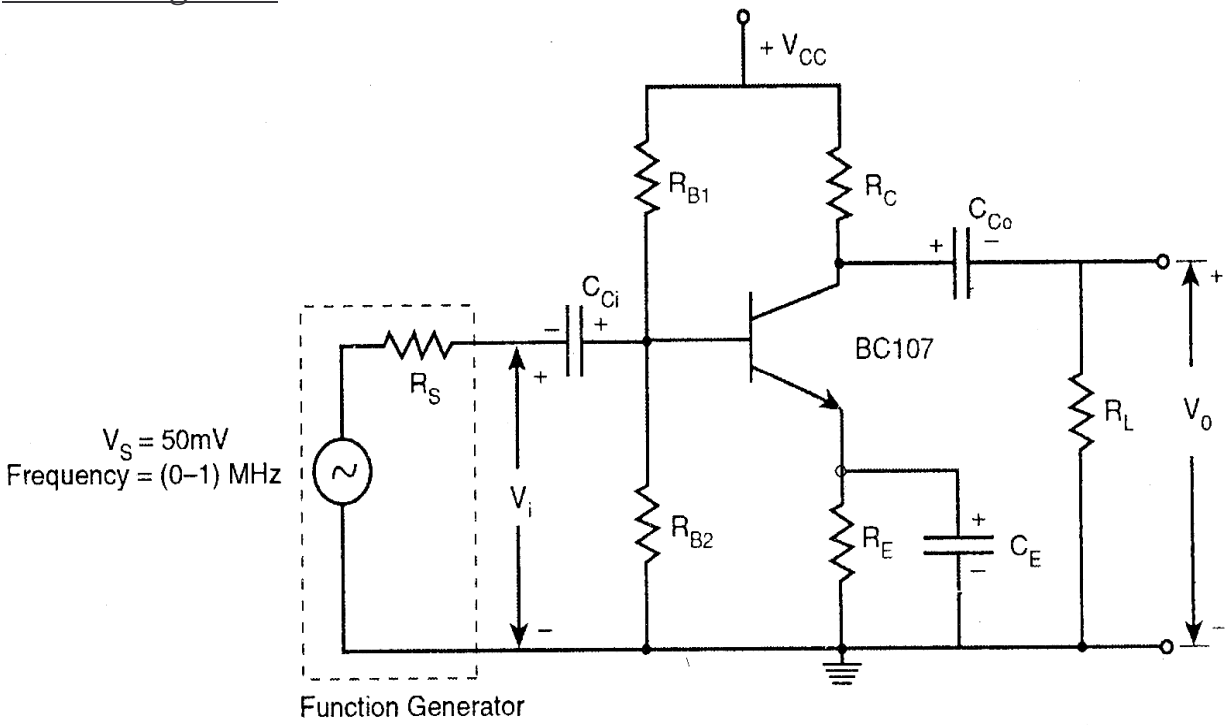
Circuit Diagram :-



Design :-

Given: $V_{CC} = 15$ V; $I_C = 1$ mA; $A_V = 50$; $f_L = 500$ Hz; Stability factor = [2–10].

Gain formula is given by,

$$A_V = \frac{-h_{fe} R_{L.eff}}{h_{ie}}$$

Assume, $V_{CE} = \frac{V_{CC}}{2}$ (Active condition); $V_E = \frac{V_{CC}}{10}$

Effective load resistance is given by $R_{Leff} = R_C \parallel R_L$.

Internal emitter resistance is given by $r_e = \frac{26\,\text{mV}}{I_E}$

$$h_{ie} = \beta r_e$$

where r_e is internal emitter resistance of the transistor.

$$h_{ie} = h_{fe}\, r_e$$

On applying KVL to output loop, we get

$$V_{CC} = I_C R_C + V_{CE} + I_E R_E$$

where

$$V_E = I_E R_E$$

$$R_C = ?$$

Experiment No: DATE: __/__/____

RC COUPLED AMPLIFIER

AIM: -To design a RC coupled single stage FET/BJT amplifier and determination of the gain-frequency response, input and output impedances.

APPARATUS REQUIRED:-

Transistor - BC 107, capacitors, resistor, power supply, CRO, function generator, multimeter, etc.

PROCEDURE: -

1. Connect the circuit as per the circuit diagram.
2. Set Vs = 50mV (assume) using the signal generator
3. Keeping the input voltage constant, vary the frequency from 0Hz to 1MHz in regular steps of 10 and note down corresponding output voltage.
4. Plot the frequency response: Gain (dB) vs Frequency (Hz).
5. Find the input and output impedance.
6. Calculate the bandwidth from the graph.
7. Note down the phase angle, bandwidth, input and output impedance.

The emitter current is given by the equation $I_E = I_B + I_C$

Since I_B is very small when compared with I_C,

$$I_C \approx I_E$$

$$R_E = \frac{V_E}{I_E} = ?$$

The voltage at the base of the transistor is given by

$$V_B = V_{BE} + V_E$$

From voltage divider rule, the voltage at the base of the transistor is given by

$$V_B = V_{CC} \frac{R_{B2}}{R_{B1} + R_{B2}}$$

The equation for stability factor is given by

$$S = 1 + \frac{R_B}{R_E}$$

Find R_B

$$R_B = R_{B1} \parallel R_{B2}$$

From equations (i) and (ii), solve for R_{B1}, and R_{B2}

Input coupling capacitor is given by,

$$X_{Ci} = \frac{(h_{ie} \parallel R_B)}{10}$$

$$X_{Ci} = \frac{1}{2\pi f C_i}$$

$$C_i = ?$$

Output coupling capacitor is given by

$$X_{C0} = \frac{R_C \parallel R_L}{10}$$

$$X_{C0} = \frac{1}{2\pi f C_0}$$

$$C_0 = ?$$

By-pass capacitor is given by, $X_{CE} = \frac{R'_E}{10}$

where,

$$R'_E = \left[R_E \parallel \frac{(R_B + h_{ie})}{h_{fe}} \right]$$

$$X_{CE} = \frac{1}{2\pi f C_E}$$

$$C_E = ?$$

General Procedure for Calculation :-

1. Input impedance

a. Connect a Decade Resistance Box (DRB) between input voltage source and the base of the transistor (series connection).

b. Connect ac voltmeter (0-100mV) across the biasing resistor R_2.

c. Vary the value of DRB such that the ac voltmeter reads the voltage half of the input signal.

d. Note down the resistance of the DRB, which is the input impedance.

2. Output impedance

a. Measure the output voltage when the amplifier is operating in the mid-band frequency with load resistance connected (V_{load}).

b. Measure the output voltage when the amplifier is operating in the mid-band frequency without load resistance connected ($V_{no\text{-}load}$).

c. Substitute these values in the formula $Z_O = \frac{V_{load} - V_{no-load}}{V_{load}} \times 100\%$

3. Bandwidth

a. Plot the frequency response

b. Identify the maximum gain region.

c. Drop a horizontal line bi –3dB.

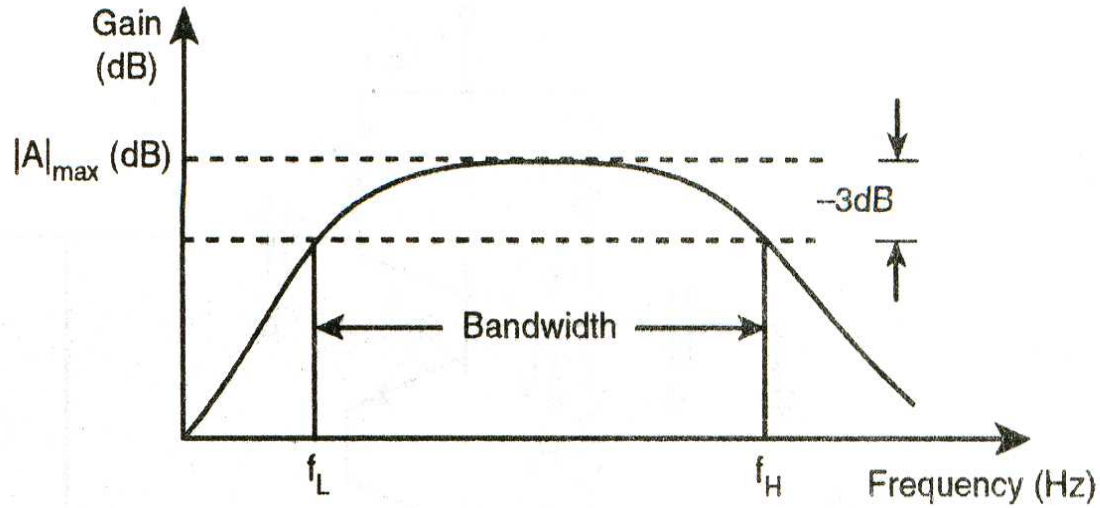
d. The –3dB line intersects the frequency response plot at two points.

e. The lower intersecting point of –3dB line with the frequency response plot gives the lower cut-off frequency.

f. The upper intersecting point of –3dB line with the frequency response plot gives the upper cut-off frequency.

g. The difference between upper cut-off frequency and lower cut-off frequency is called Bandwidth. Thus Bandwidth = $f_h - f_l$.

Model Graph (Frequency Response) :-



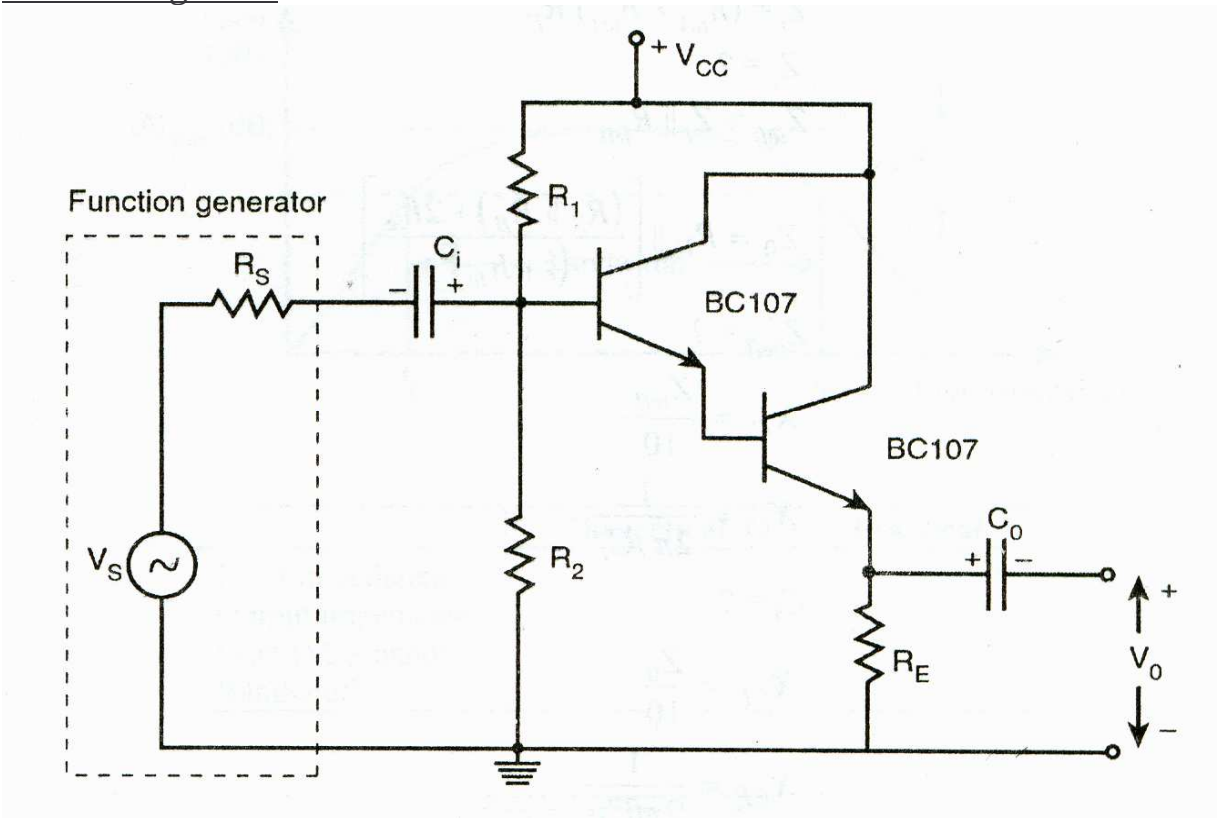
TABULAR COLUMN : -

Sl No.	Frequency	V_O (volts)	Gain = V_O/V_i	Gain (dB) =20log V_O/V_i

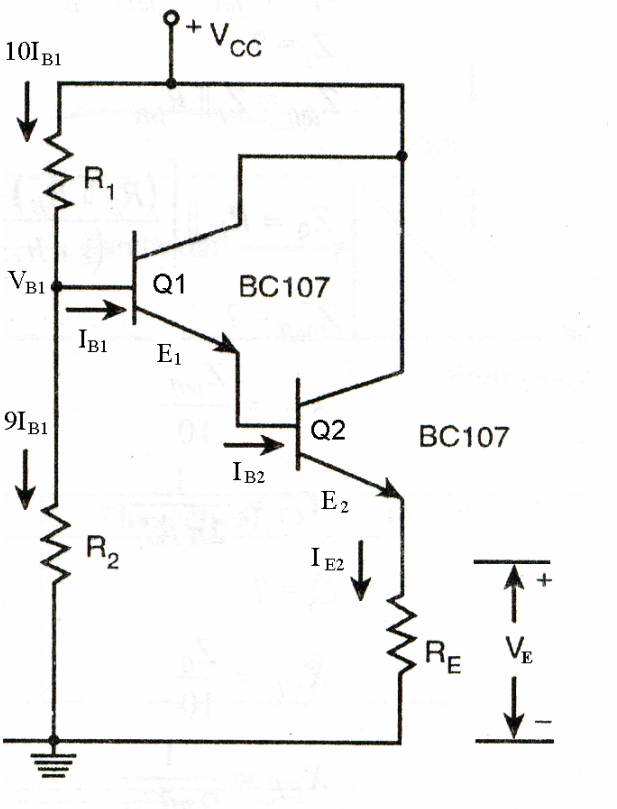
Result :-

	Theoretical	**Practical**
Input impedance		
Output impedance		
Gain (Mid band)		
Bandwidth		

Circuit Diagram :-



DC Analysis :-



Experiment No: **DATE: __/__/____**

DARLINGTON EMITTER FOLLOWER

AIM: - To design a BJT Darlington Emitter follower and determine the gain, input and output impedances.

APPARATUS REQUIRED:-

Transistor - BC 107, capacitors, resistor, power supply, CRO, function generator, multimeter, etc.

PROCEDURE: -

1. Connect the circuit as per the circuit diagram.
2. Set V_i = 1 volt (say), using the signal generator
3. Keeping the input voltage constant, vary the frequency from 0Hz to 1MHz in regular steps of 10 and note down corresponding output voltage.
4. Plot the frequency response: Gain (dB) vs Frequency (Hz).
5. Find the input and output impedance.
6. Calculate the bandwidth from the graph.
7. Note down the phase angle, bandwidth, input and output impedance.

Design :-

Given $V_{CEQ} = V_{CE2} = 6v$

$I_{CQ} = I_{C2} = 5mA$

Assume β for SL100 = 100

$V_{CC} = 12v$

$V_{E2} = \frac{V_{CC}}{2} = \frac{12}{2} = 6v$

$I_{E2}R_E = V_{E2}$

$\therefore R_E = \frac{V_{E2}}{I_{E2}} = \frac{6}{5\times10^{-3}} = 1.2k\Omega \ [\because IE_2 = IC_2]$

$\therefore R_E = 1.2k\Omega$

$VB_1 = VBE_1 + VBE_2 + VE_2$

$VB_1 = 0.7 + 0.7 + 6$

$VB_1 = 7.4v$

$IB_2 = \frac{I_{C2}}{\beta} = \frac{5\times10^{-3}}{100} = 0.05mA$

$IB_1 = \frac{I_{C1}}{\beta} = \frac{I_{B2}}{\beta} = \frac{0.05}{100} = 0.0005mA$

$10IB_1R_1 = V_{CC} - VB_1$

$\therefore R_1 = \frac{12 - 7.4}{10\times0.0005\times10^{-3}} = 920k\Omega \ [\text{Use } R_1 = 1M\Omega]$

$R_2 = \frac{V_{B1}}{9I_B} = 1644k\Omega$

$\therefore R_2 = 1.5M\Omega$

General Procedure for Calculation:

1. Input impedance

a. Connect a Decade Resistance Box (DRB) between input voltage source and the base of the transistor (series connection).

b. Connect ac voltmeter (0-100mV) across the biasing resistor R_2.

c. Vary the value of DRB such that the ac voltmeter reads the voltage half of the input signal.

d. Note down the resistance of the DRB, which is the input impedance.

2. Output impedance

a. Measure the output voltage when the amplifier is operating in the mid-band frequency with load resistance connected (V_{load}).

b. Measure the output voltage when the amplifier is operating in the mid-band frequency without load resistance connected ($V_{no\text{-}load}$).

c. Substitute these values in the formula $Z_O = \frac{V_{load} - V_{no-load}}{V_{load}} \times 100\%$

3. Bandwidth

a. Plot the frequency response

b. Identify the maximum gain region.

c. Drop a horizontal line bi –3dB.

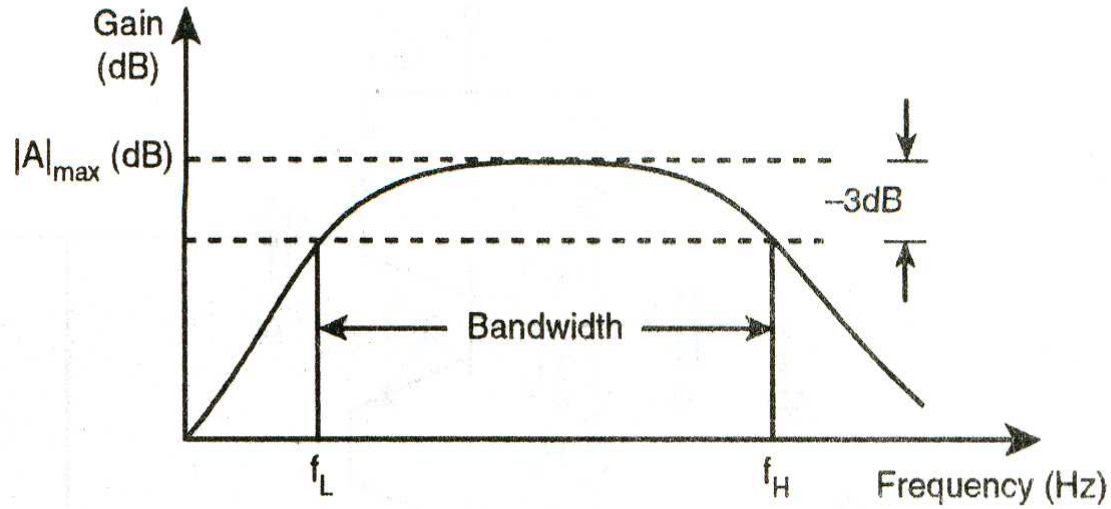
d. The –3dB line intersects the frequency response plot at two points.

e. The lower intersecting point of –3dB line with the frequency response plot gives the lower cut-off frequency.

f. The upper intersecting point of –3dB line with the frequency response plot gives the upper cut-off frequency.

g. The difference between upper cut-off frequency and lower cut-off frequency is called Bandwidth. Thus Bandwidth = $f_h - f_l$.

Model Graph: (Frequency Response)



TABULAR COLUMN: -

Sl No.	Frequency	V_O (volts)	Gain = V_O/V_i	Gain (dB) =20log V_O/V_i

4. To find Q-Point

a. Connect the circuit as per circuit diagram

b. Switch on the DC source [switch off the AC source]

c. Measure voltage at V_{B2}, V_{E2} & V_{C2} with respect to ground

& also measure

$$V_{CE2} = V_{C2} - V_{E2}$$

$$I_{C2} = I_{E2} = \frac{V_{E2}}{R_E}$$

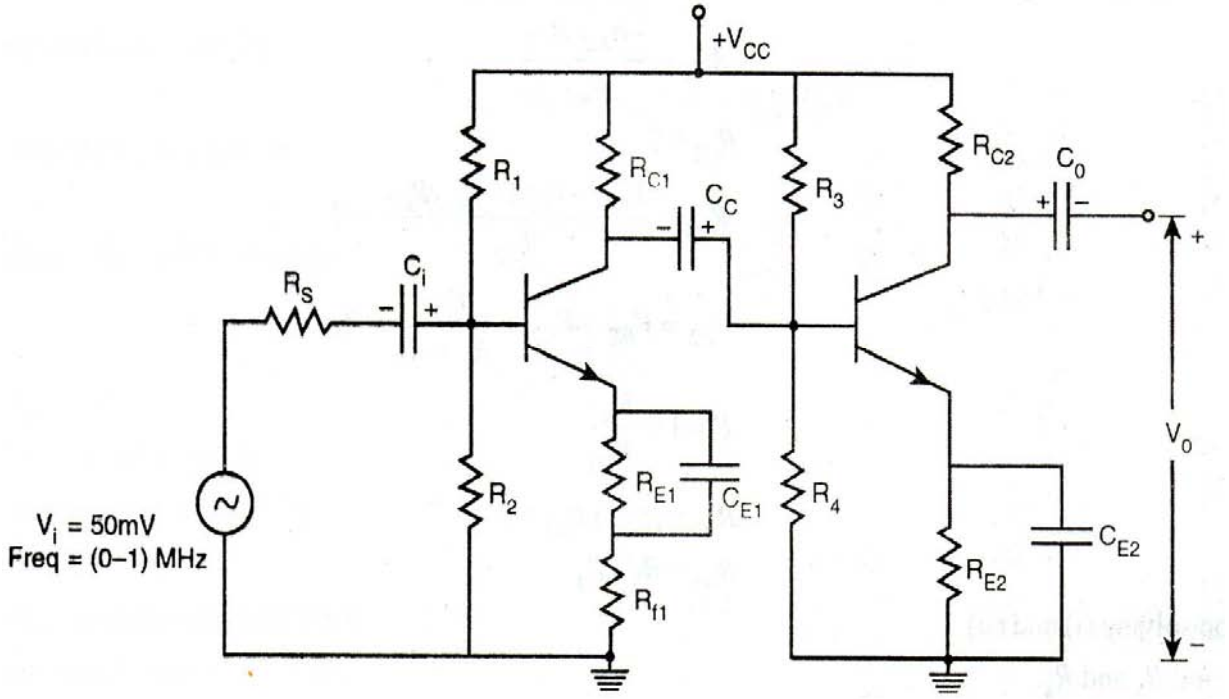
$$Q - Point = [V_{CE2}, I_{C2}]$$

Result

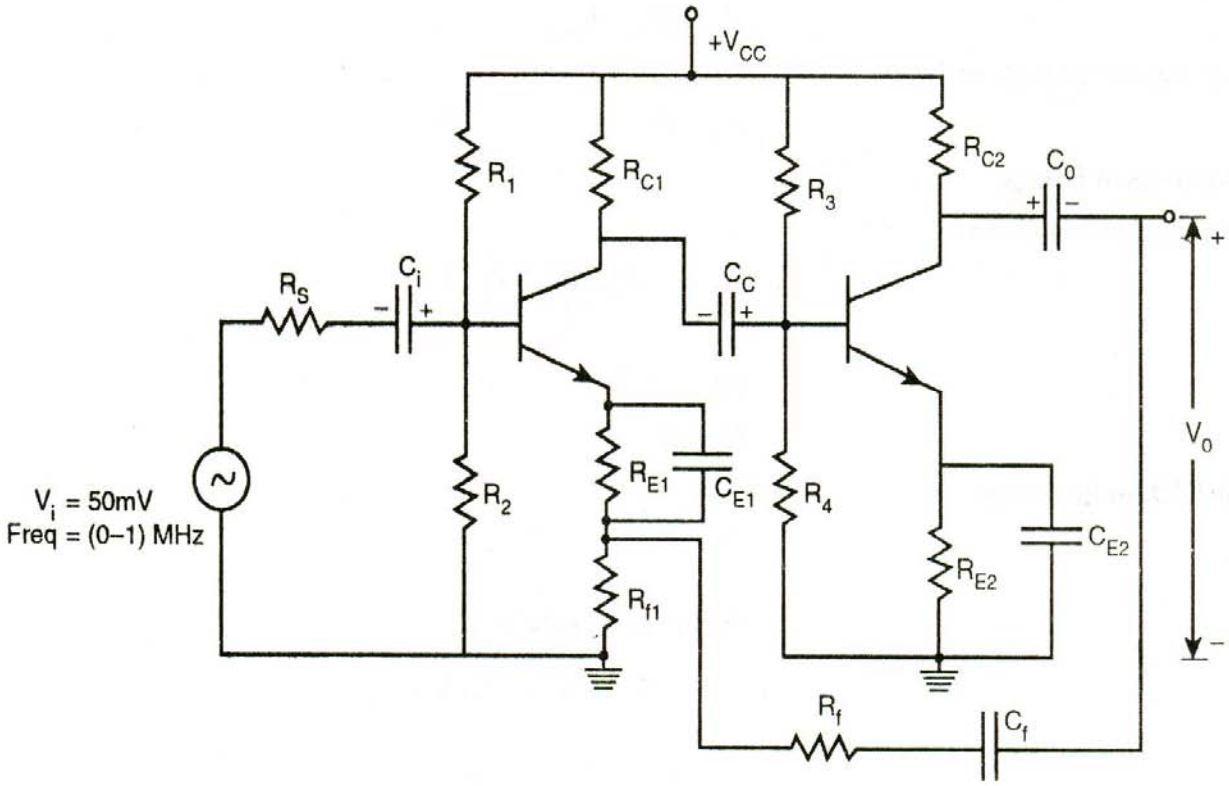
	Theoretical	**Practical**
Input impedance		
Output impedance		
Gain (Mid band)		
Bandwidth		

Circuit Diagram :-

Amplifier without Feedback



Amplifier with Feedback



Experiment No: **DATE: __/__/____**

VOLTAGE SERIES FEEDBACK AMPLIFIER

AIM: - To design a FET/BJT Voltage series feedback amplifier and determine the gain, frequency response, input and output impedances with and without feedback

APPARATUS REQUIRED:-

Transistor - BC 107, capacitors, resistor, power supply, CRO, function generator, multimeter, etc.

PROCEDURE: -

1. Connect the circuit as per the circuit diagram.
2. Set Vs = 50mV (assume) using the signal generator
3. Keeping the input voltage constant, vary the frequency from 0Hz to 1MHz in regular steps of 10 and note down corresponding output voltage.
4. Plot the frequency response: Gain (dB) vs Frequency (Hz).
5. Find the input and output impedance.
6. Calculate the bandwidth from the graph.
7. Note down the phase angle, bandwidth, input and output impedance.

Design (With Feedback):-

Given $A_{V1} = 30$; $A_{12} = 20$; $V_{CC} = 10V$; $I_{E2} = 1.8mA$; $I_{E1} = 1.1mA$; $S = 3$; h_{fe1} and h_{fe2} are obtained by multimeter $\beta = 0.03$

DC Analysis of II Stage: -

$$V_{CC} = I_{C2}R_{C2} + V_{CE2} + I_{E2}R_{E2}$$

$$R_{B1} = (S-1)\,R_{E1} = ?$$

$$R_{B1} = R_1 \parallel R_2$$

find R_1 and R_2

Input impedance is given by

$$Z_{i1} = R_{B1} \parallel [h_{ie1} + (1 + h_{fe1})\,R_{f1}]$$

Output impedance is given by

$$Z_{o1} = R_{C1}$$

The feedback factor β is given by

$$\beta = \frac{R_{f1}}{R_{f1} + R_{f2}}$$

where, $R_{f2} >> R_{f1}$

assume $R_{f2} = 10\ k\Omega$; find R_{f1}

overall voltage gain is given by

$$A_V = A_{V1} \times A_{V2}$$

Parameter Analysis with Feedback

The desensitive factor, $D = 1 + \beta A_V$

Output impedance with feedback is given by

$$Z_{of} = \frac{Z_{o2}}{D}$$

Input impedance with feedback is given by

$$Z_{if} = Z_{i1} \times D$$

The gain with feedback is given by

$$A_{Vf} = \frac{A_V}{D}$$

The output capacitor is given by

$$X_{C0} = \frac{Z_{o2}}{10}$$

where $X_{C0} = \frac{1}{2\pi f C_0}$

$C_0 = ?$

The input capacitor is given by,

$$X_{Ci} = \frac{Z_{i1}}{10}$$

where $X_{Ci} = \frac{1}{2\pi f_{Ci}}$

$C_i = ?$

for active condition, $V_{CE2} = \frac{V_{CC}}{2}$

The voltage gain is given by

$$A_{V2} = \frac{-h_{fe2} R_{C2}}{h_{ie2}}$$

$R_{C2} = ?$

$$R_{E2} = \frac{V_{CC} - V_{CE2} - I_{C2}R_{C2}}{I_{E2}} = ?$$

$$V_{B2} = V_{BE} + V_{E2} = \frac{V_{CC}}{R_3 + R_4} \times R_4$$

$$S = 1 + \frac{R_{B2}}{R_{E2}}$$

$R_{B2} = (S-1)\, R_{E2} = ?$

$R_{B2} = R_3 \parallel R_4$

on solving (i) and (ii)

Find R_3 and R_4.

Input impedance is given by,

$$Z_{i2} = (R_{B2} \parallel h_{ie2})$$

Output impedance is given by,

$$Z_{o2} = R_{C2}$$

DC Analysis of *I* Stage

The voltage gain is given by

$$A_{V1} = \frac{-h_{fe1}(R_{C1} \parallel Z_{iC})}{h_{ie1}}$$

$(R_{C1} \parallel Z_{i2}) = ?$

Find $R_{C1} = ?$

Apply KVL to first stage,

$$V_{CC} = I_{C1} R_{C1} + V_{CE1} + I_{E1} R_{E1}$$

for active condition, $V_{CE1} = \frac{V_{CC}}{2}$

$$V_{E1} = \frac{V_{CC} - V_{CE1} - I_{C1} R_{C1}}{I_{E1}} = ?$$

$$V_{B1} = V_{BE} + V_{E1} = \frac{V_{CC}}{R_1 + R_2} \times R_2$$

$$S = 1 + \frac{R_{B1}}{R_{E1}}$$

The emitter capacitor of first stage is given by

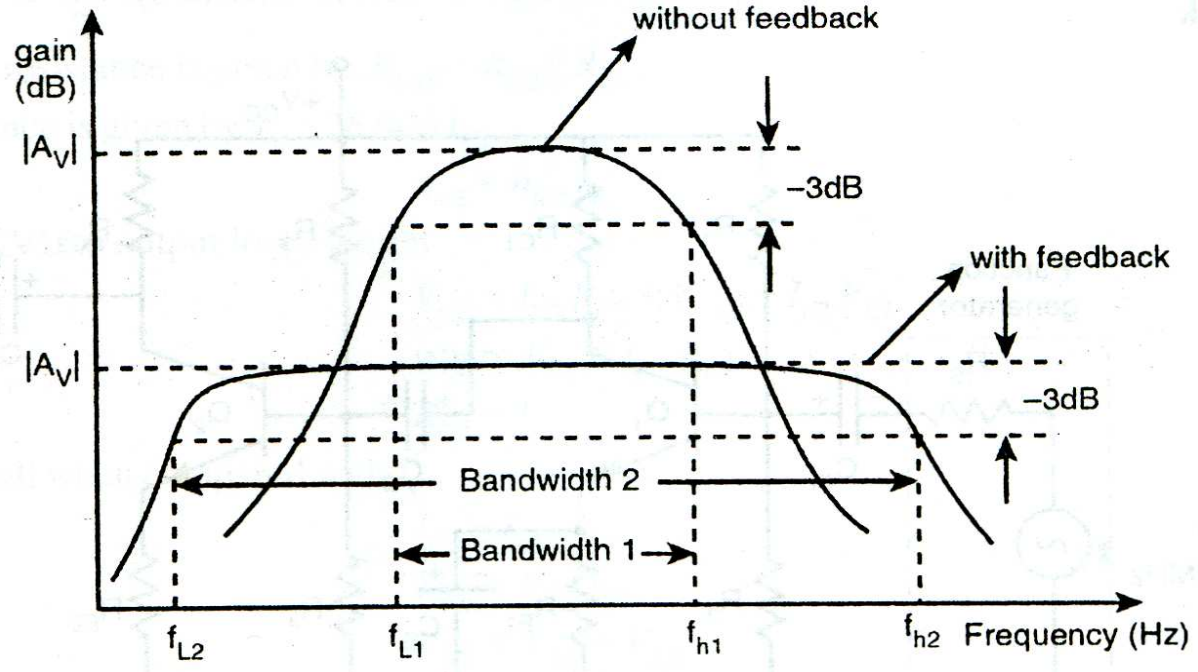
$$X_{CE} = \frac{R'_{E1}}{10} \text{ where } R'_{E1} = R_E \parallel \left\{ R_{f1} + \left(\frac{R_{B1} + h_{ie2}}{1 + h_{fe2}} \right) \right\}$$

The emitter capacitor of II stage is given by

$$X_{CE2} = \frac{R'_{E2}}{10}$$

$$\text{where } R'_{E2} = R_{E2} \parallel \left(\frac{h_{ie2} + R_{B2}}{1 + h_{fe2}} \right)$$

Model Graph (Frequency Response) :-



General Procedure for Calculation:

1. Input impedance

a. Connect a Decade Resistance Box (DRB) between input voltage source and the base of the transistor (series connection).

b. Connect ac voltmeter (0-100mV) across the biasing resistor R_2.

c. Vary the value of DRB such that the ac voltmeter reads the voltage half of the input signal.

d. Note down the resistance of the DRB, which is the input impedance.

2. Output impedance

a. Measure the output voltage when the amplifier is operating in the mid-band frequency with load resistance connected (V_{load}).

b. Measure the output voltage when the amplifier is operating in the mid-band frequency without load resistance connected ($V_{no\text{-}load}$).

c. Substitute these values in the formula $Z_O = \frac{V_{load} - V_{no-load}}{V_{load}} \times 100\%$

3. Bandwidth

a. Plot the frequency response

b. Identify the maximum gain region.

c. Drop a horizontal line bi –3dB.

d. The –3dB line intersects the frequency response plot at two points.

e. The lower intersecting point of –3dB line with the frequency response plot gives the lower cut-off frequency.

f. The upper intersecting point of –3dB line with the frequency response plot gives the upper cut-off frequency.

g. The difference between upper cut-off frequency and lower cut-off frequency is called Bandwidth. Thus Bandwidth = $f_h - f_l$.

TABULAR COLUMN: -

With Feedback (V_i = 50mV)

Sl No.	Frequency	V_O (volts)	Gain = V_O/V_i	Gain (dB) =20log V_O/V_i

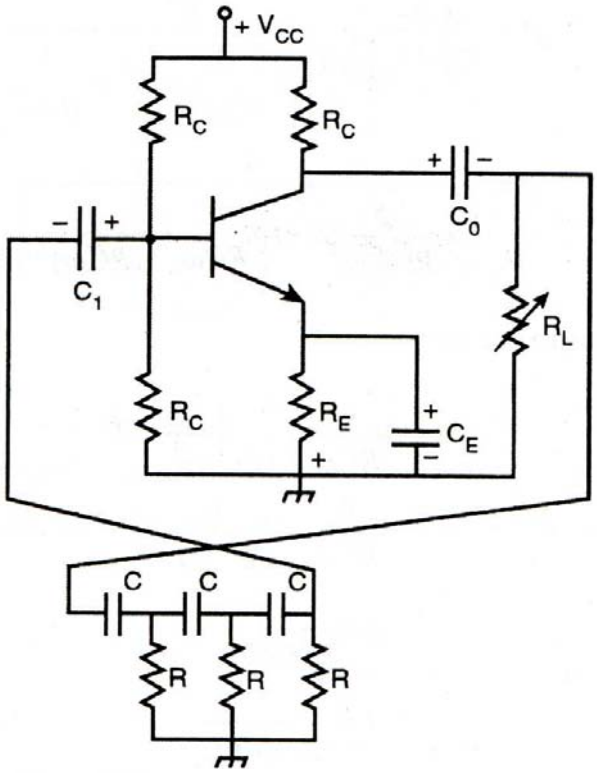
Without Feedback (V_i = 50mV)

Sl No.	Frequency	V_O (volts)	Gain = V_O/V_i	Gain (dB) =20log V_O/V_i

Result

	Theoretical		**Practical**	
	With f/b	**Without f/b**	**With f/b**	**Without f/b**
Input impedance				
Output impedance				
Gain (Mid band)				
Bandwidth				

Circuit Diagram :-



Design

Given $f_0 = 1$ kHz; $C = 0.01$ μF, $V_{CC} = 12$ V

$$f = \frac{1}{2\pi\sqrt{6}RC}$$

Find R

$$\beta(s) = -\frac{1}{29}$$

$$A = \frac{1}{\beta} = -29$$

Amplifier Design

Gain formula is given by,

$$A_V = \frac{-h_{fe}R_{Leff}}{h_{ie}} \quad (A_V = 29, \text{ design given})$$

Assume $V_{CE} = V_{CC}/2$ (transistor Active)

Effective load resistance is given by, $R_{\text{Leff}} = R_C || R_L$

Emitter resistance is given by, $R_E = 26\text{m V}/I_E$

$$h_{ie} = \beta r_e$$

Where r_e is internal resistance of the transistor.

$$h_{ie} = h_{fe} r_e$$

$$V_E = V_{CC}/10$$

Experiment No: **DATE: __/__/____**

RC PHASE SHIFT OSCILLATOR

AIM: - To design And test for the performance of RC Phase Shift Oscillator for the given operating frequency f_O.

APPARATUS REQUIRED:-

Transistor - BC 107, capacitors, resistor, power supply, CRO, multimeter, etc.

PROCEDURE: -

1. Connect the circuit as per the circuit diagram (both oscillators).
2. Switch on the power supply and observe the output on the CRO (sine wave).
3. Note down the practical frequency and compare with its theoretical frequency.

on applying KVL to output loop, we get

$$V_{CC} = I_C R_C + V_{CE} + I_E R_E$$

where $V_E = I_E R_E$

Find R_C

Since I_B is very small when compare with I_C,

$$I_C \approx I_E$$

$$R_E = V_E / I_E$$

$$V_B = V_{BE} + V_E$$

$$V_B = V_{CC} \frac{R_{B2}}{R_{B1} + R_{B2}}$$

$$S = 1 + \frac{R_B}{R_E}$$

Find R_B

$$R_B = R_{B1} \parallel R_{B2}$$

Find R_{B1} and R_{B2}

Coupling and by-pass capacitors can be found out by,

Input coupling capacitor is given by, $X_{Ci} = \{[h_{ie} + (1 + h_{fe}) R_E] \parallel R_B\} / 10$

$$X_{Ci} = \frac{1}{2\pi f C_i}$$

Find C_i

$$X_{C0} = \frac{1}{2\pi f C_0}$$

Find C_0

By-pass capacitor is given by, $X_{CE} = R_E / 10$

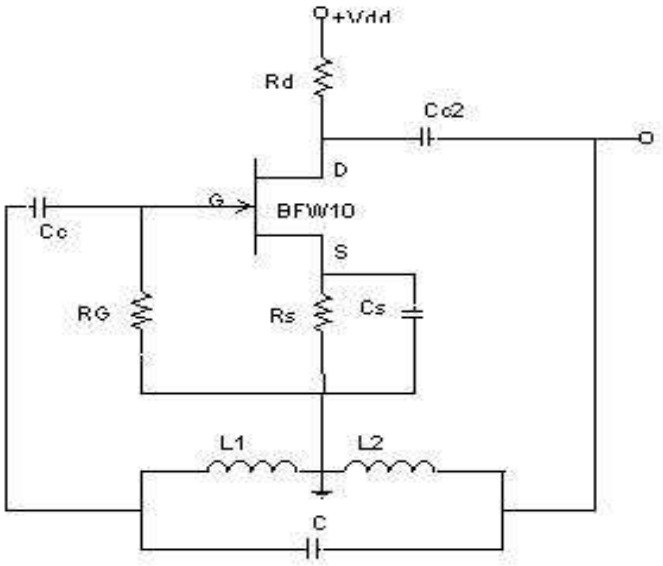
$$X_E = \frac{1}{2\pi f C_E}$$

Find C_E

Result

	Theoretical	Practical
Frequency		

HARTLEY OSCILLATOR:-



DESIGN:-

$f = \frac{1}{2\Pi\sqrt{LC}}$, where L=L1+L2

Assume $\frac{L2}{L1} = 5$, Let L1=2mH $\therefore$ L2=10mH

Let Vgs =-1.5V, $\therefore$ Id =Idss $(1 - \frac{Vgs2}{Vp}) = 3mA$

$g_m = \frac{-2Idss}{Vp}(1 - \frac{Vgs}{Vp}) = 4mmhos$

$\therefore RS = \frac{Vs}{Id} = \frac{-Vgs}{Id} = \frac{1.5}{3m} = 500\Omega$

Assume Av =10 $(> \frac{L2}{L1}) \Rightarrow 10 = g_m.Rd$

$\therefore Rd = \frac{10}{4m} = 2.5K\Omega$

Assume Rg =1MΩ, Cc1=Cc2=0.1μf,Cs=47 μf,

Assuming Vds=5V

$\therefore$ Vdd = IdRd+Vds+Vs=14V

Experiment No: **DATE: __/__/____**

HARTLEY AND COLPITTS OSCILLATOR

AIM:- To design and test for the performance of FET – Hartley & Colpitt's Oscillators.

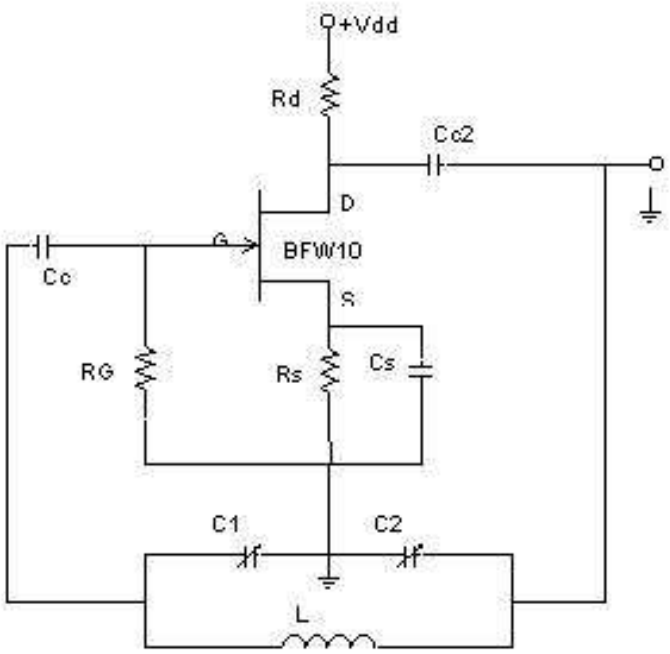
APPARATUS REQUIRED:-

Transistor – BFW10, capacitors, resistor, power supply, CRO, function generator, multimeter, etc.

PROCEDURE: -

1. Connect the circuit as per the circuit diagram (both oscillators).
2. Switch on the power supply and observe the output on the CRO (sine wave).
3. Note down the practical frequency and compare with its theoretical frequency.

COLPITTS OSCILLATOR:-



DESIGN:-

$f = \frac{1}{2\Pi\sqrt{LC}}$, where $C\frac{C1C21}{C1+C2}$

Assume $\frac{C1}{C2} = 5$, Let C1=500pF $\therefore$ C2=100pF

$\therefore$ L =0.12H, for f=50KHz

Let Vgs =-1.5V, $\therefore$ Id=Id =Idss$1-\frac{Vgs2}{Vp}) = 3mA$

$g_m = \frac{-2Idss}{Vp} = \frac{-Vgs}{Vp} = 4mmhos$

$\therefore Rs = \frac{Vs}{Id} = \frac{-Vgs}{Id} = \frac{1.5}{3m} = 500\Omega$

Assume Av =10 $(> \frac{C1}{C2}) \Rightarrow 10 = g_{m}.Rd$

$\therefore Rd = \frac{10}{4m} = 2.5K\Omega$

Assume Rg =1MΩ, Cc1=Cc2=0.1μf,Cs=47 μf,

assuming Vds=5V

$\therefore$ Vdd = IdRd+Vds+Vs=14V

DESIGN:-

$$f = 1\ MHZ = \frac{1}{2\Pi\sqrt{LC}}$$

Assume L=.33H, $\therefore$ C=0.0767pF

Let Vce = 6V, Ic = 2mA,

Choose Vcc –2 Vce

$$\text{Assume Ve} = \frac{Vcc}{10} = 1.2V$$

$$\therefore \text{Re} = \frac{\text{Ve}}{\text{Ie}} \approx \frac{\text{Ve}}{\text{Ic}} = 1.2\text{V}$$

$$\therefore \text{Re} = \frac{\text{Ve}}{\text{Ie}} \approx \frac{\text{Ve}}{\text{Ic}} = \frac{1.2}{2\text{m}} = 600\Omega$$

$$\therefore \text{R1} = 34\text{K}\Omega$$

$$Rc = \frac{\text{Vcc - Cce - Vre}}{Ic1} = \frac{12 - 6 - 1.2}{2m} = 2.4K\Omega$$

Assume Cc1=Cc2=0.1μf, Ce = 47 μf,

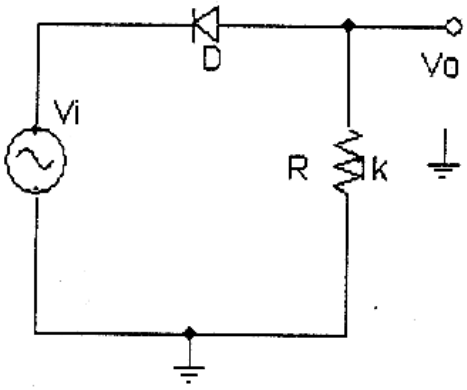
Result:-

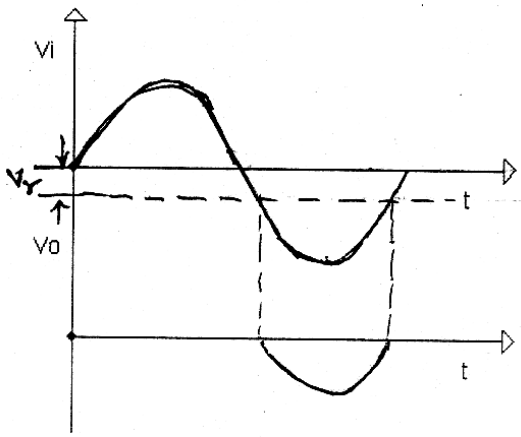
Parameter	**Theoretical**		**Practical**	
Frequency	Hartley	Colpitt	Hartley	Colpitt

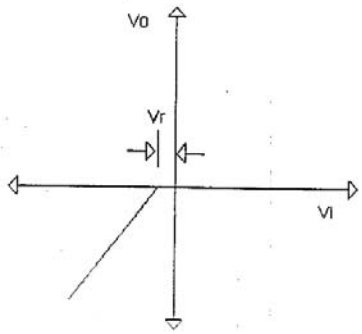
Circuit Diagram:-

Series Clippers

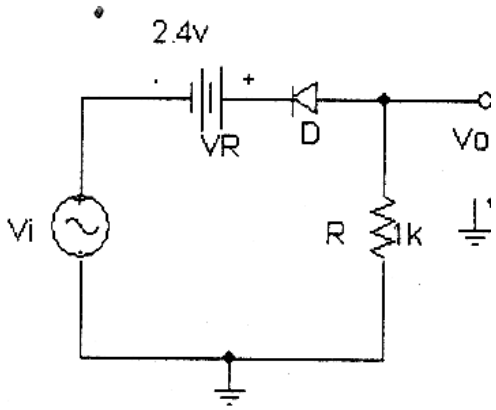
a) To pass –ve peak above Vr level :-

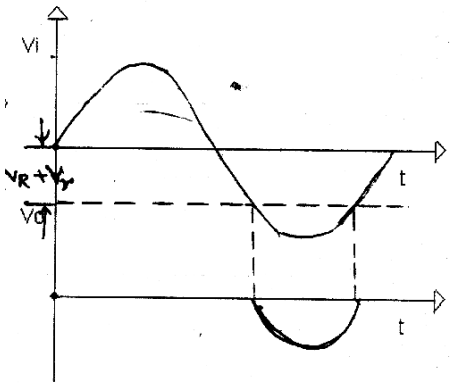


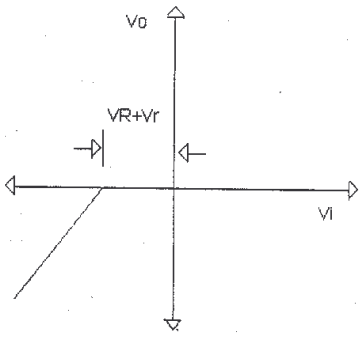




b) To pass –ve peak above some level (say –3v) :-







Experiment No: **DATE: __/__/____**

CLIPPING CIRCUITS

AIM: - To design a Clipping circuit for the given specifications and hence to plot its O/P

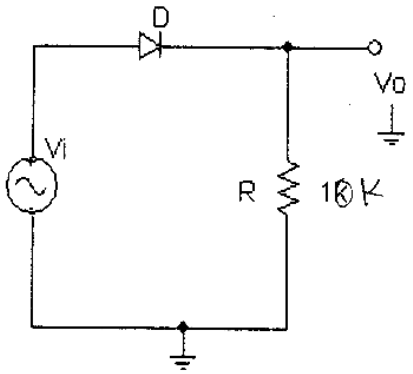
APPARATUS REQUIRED:-

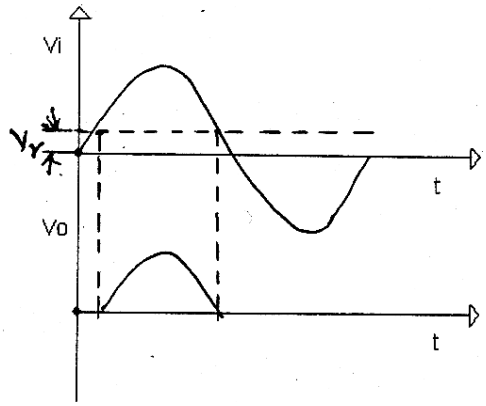
Diode-IN 4007, capacitors, resistor, power supply, CRO, function generator, multimeter, etc.

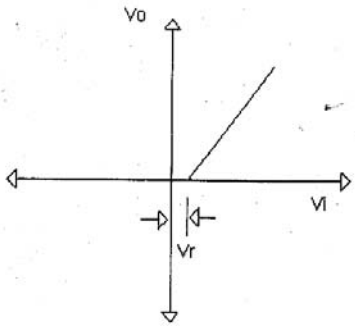
PROCEDURE: -

1. Connections are made as shown in the circuit diagram.
2. A sine wave Input Vi whose amplitude is greater than the clipping level is applied.
3. Output waveform Vo is observed on the CRO.
4. Clipped voltage is measured and verified with the designed values.

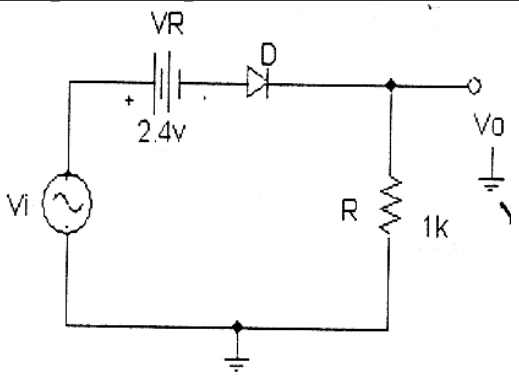
c) To pass +ve peak above Vr level :-

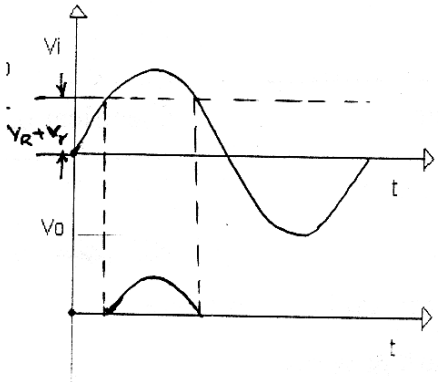


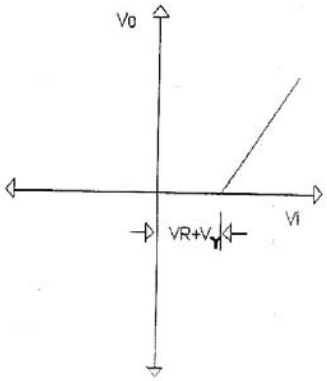




d) To pass +ve peak above some level (say +3v) :-







Design :-

Choose Rf = 10Ω, Rr = 1MΩ

$\therefore R = \sqrt{RfRr} = 3.3K\Omega$

a) To pass –ve peak above Vr level

b) To pass –ve peak above some level (say – 3v)

ie., - (VR+Vr) = -3

VR = 3-Vr

3 – 0.6 = 2.4v

c) To pass +ve peak above Vr level

d) To pass +ve peak above some level (say +3v)

ie., (VR+Vr) = +3

VR = 3-0.6 = 2.4v

e) To pass +ve peak above some level (say +4v) and –ve peak above some level (say -3v)

ie., VR+Vr = 4

VR = 3.4v

-(VR+Vr) = -3v

VR = 2.4v

f) To remove +ve peak above Vr level

g) To remove +ve peak above some level (say 3v)

ie., (VR+Vr) = 3v

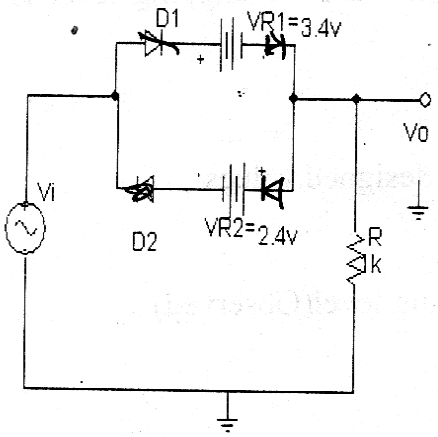
VR = 2.4v

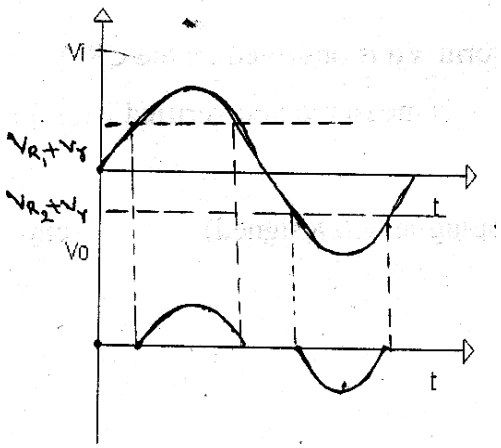
h) To pass –ve peak above some level (say -2v)

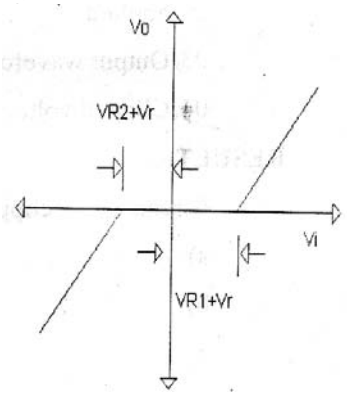
ie., -VR+Vr = -2

VR = 2.6v

e) To pass +ve peak above some level (say +4v) &
-ve peak above some level (say -3v) :-

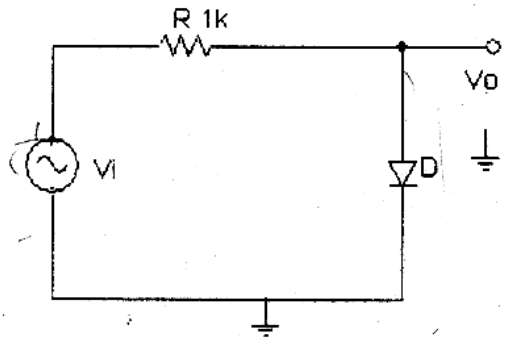


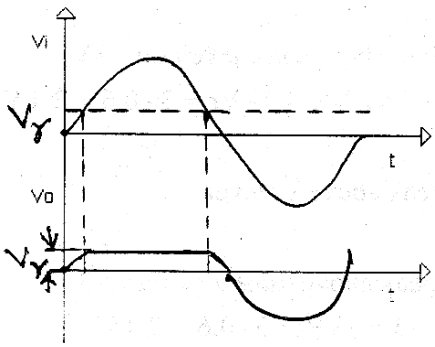


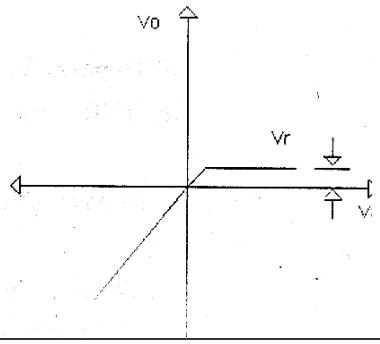


Shunt Clippers

f) To remove +ve peak above Vr level :-







i) To remove –ve peak above Vr level

j) To pass +ve peak above some level (say 2v)

ie., VR-Vr = 2

VR = 2.6v

k) To remove –ve peak above some level (say -3v)

ie., -(VR+Vr) = -3

VR = 2.4v

l) To remove +ve peak above some level (say +3v) and –ve peak above some level (say -3v)

ie., (VR1+Vr) = 3v

VR1 = 2.4v

-(VR2+Vr) = -3v

VR2 = 2.4v

m) To pass a part of the +ve half cycle (say V1 = 2v, V2 = 4.2v)

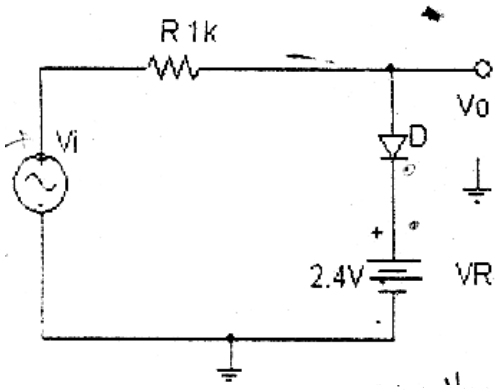
ie., (VR1 - Vr) = 2v

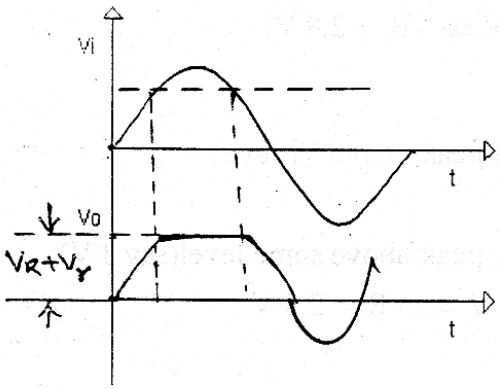
VR1 = 2.6v

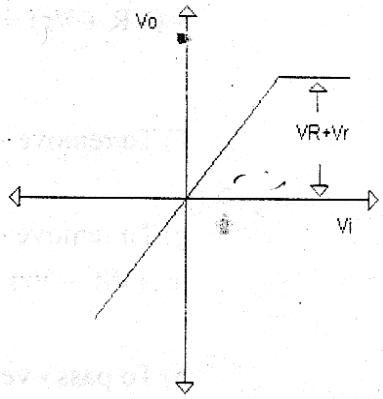
(VR2+Vr) = 4.2v

VR2 = 3.6v

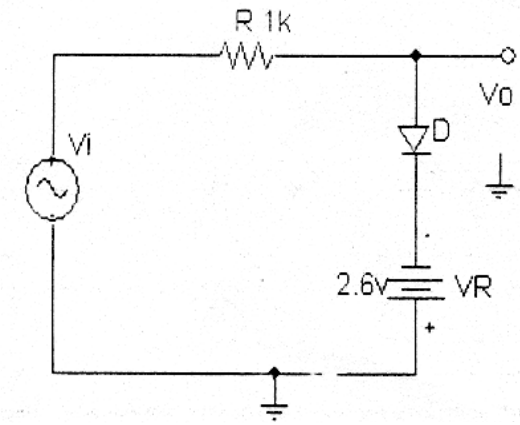
g) To remove +ve peak above some level (say +3v) :-

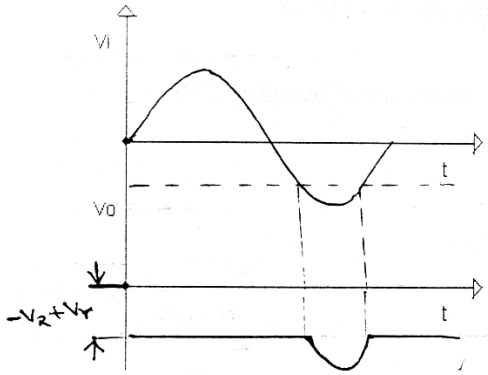


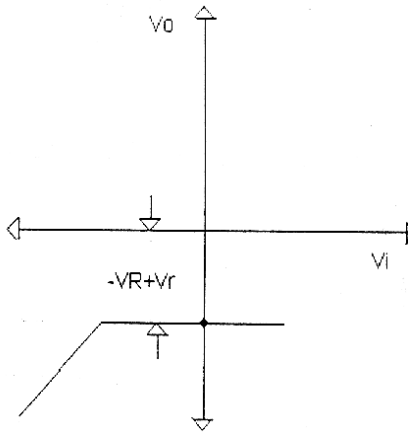




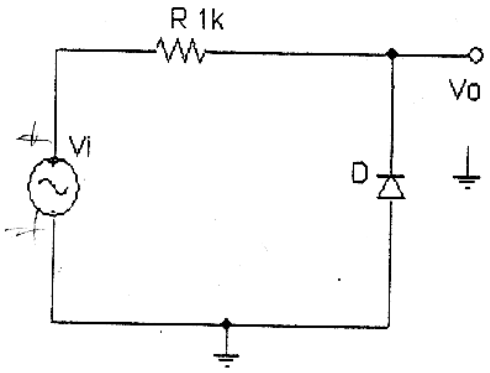
h) To pass –ve peak above some level (say -2v) :-

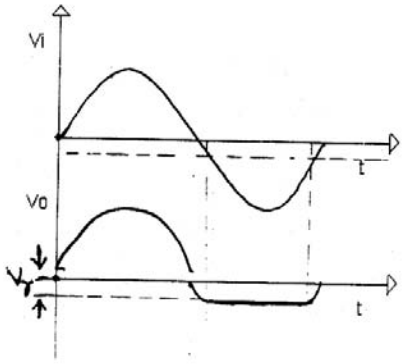


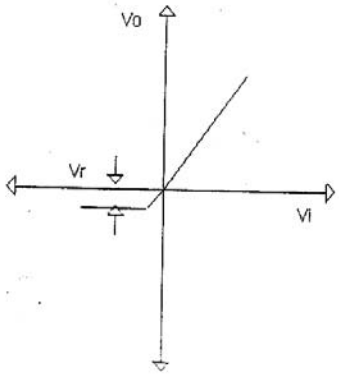




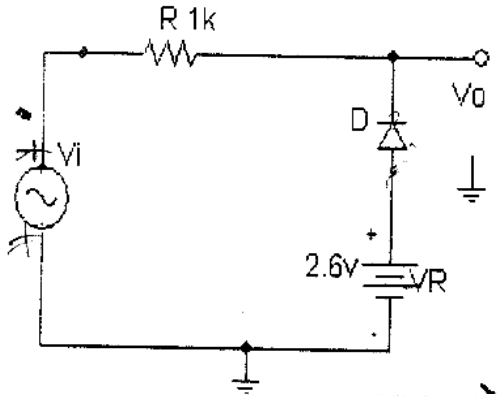
i) To remove above Vr level :-

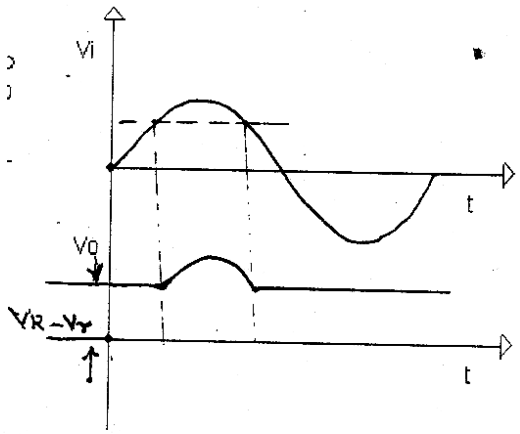


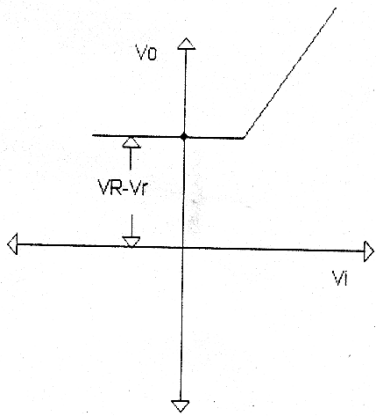




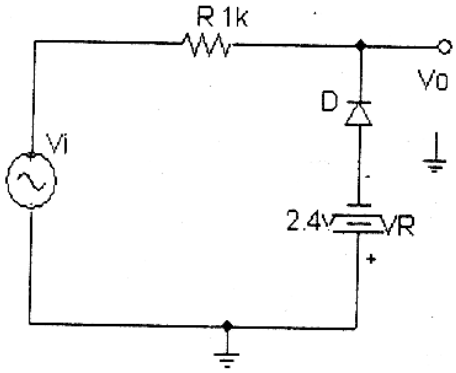
j) To pass +ve peak above some level (say +2v) :-

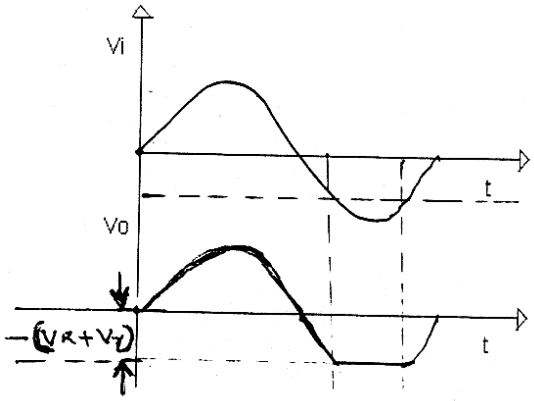


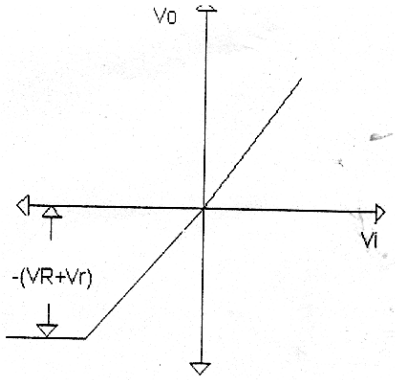




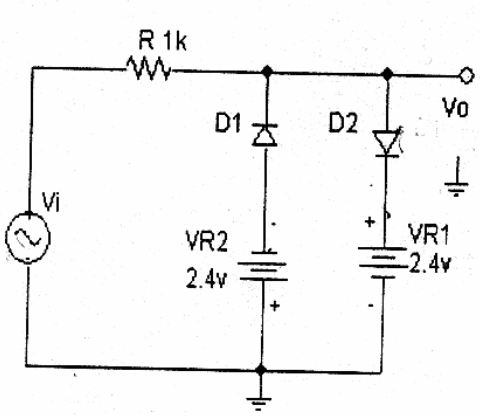
k) To remove –ve peak above some level (say -3v) :-

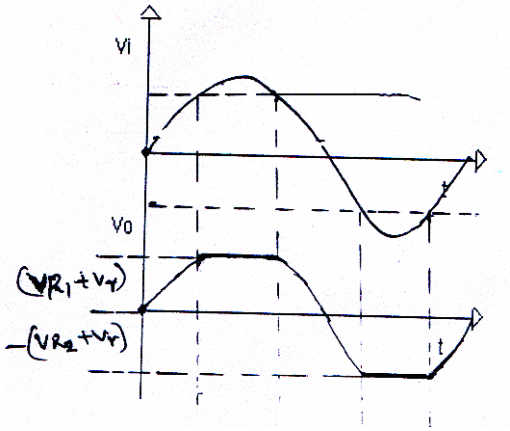


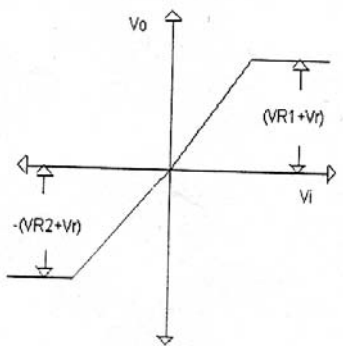




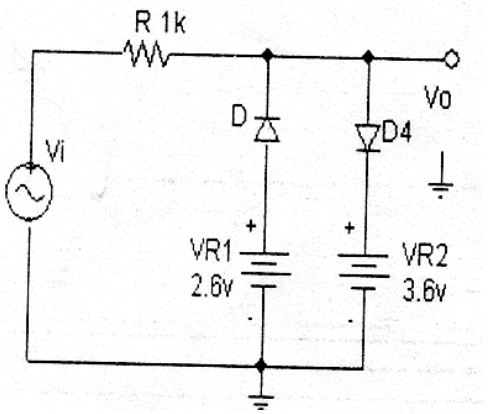
l) To remove above some level (say +3v) and -ve peak above some level (say -3v) :-

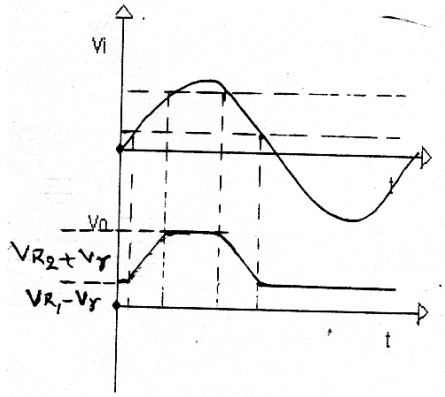


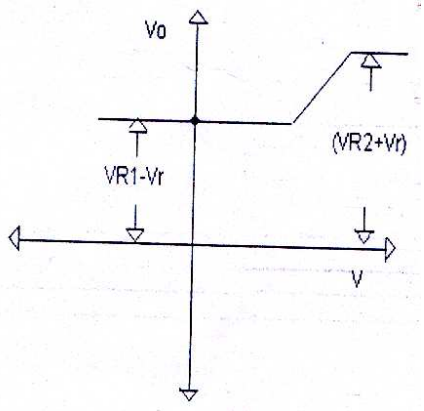




m) To pass a part of the =ve half cycle (say V1 = 2v, V2 = 4.2v) :-

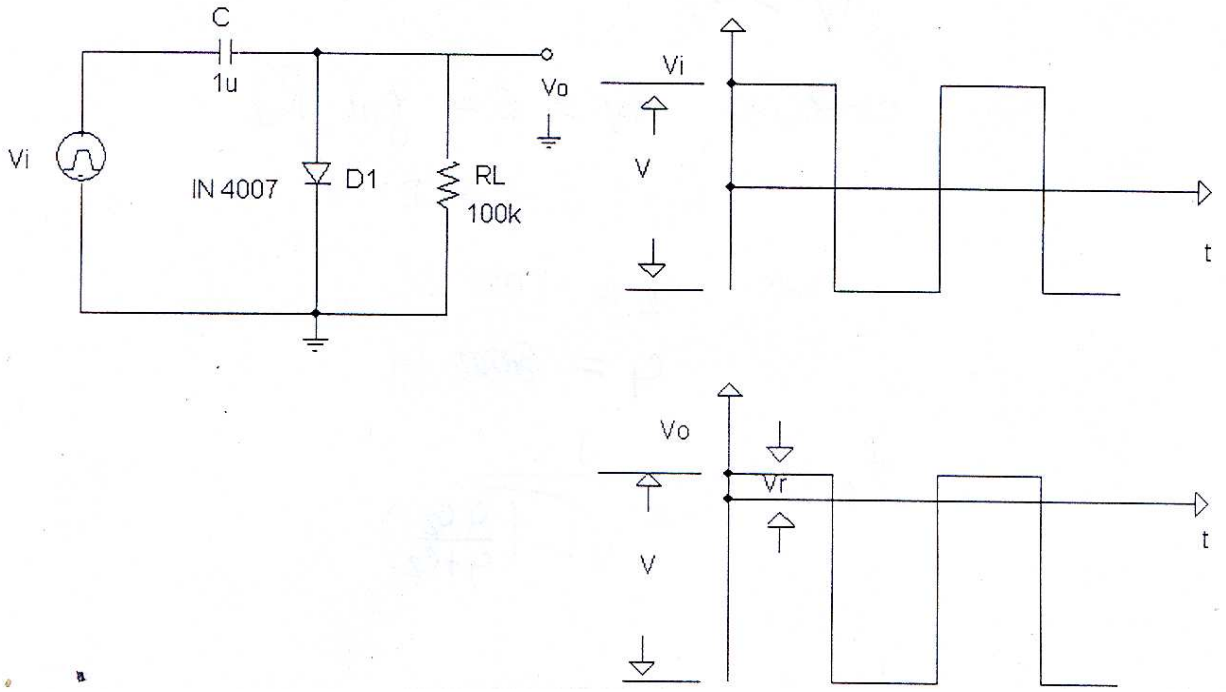




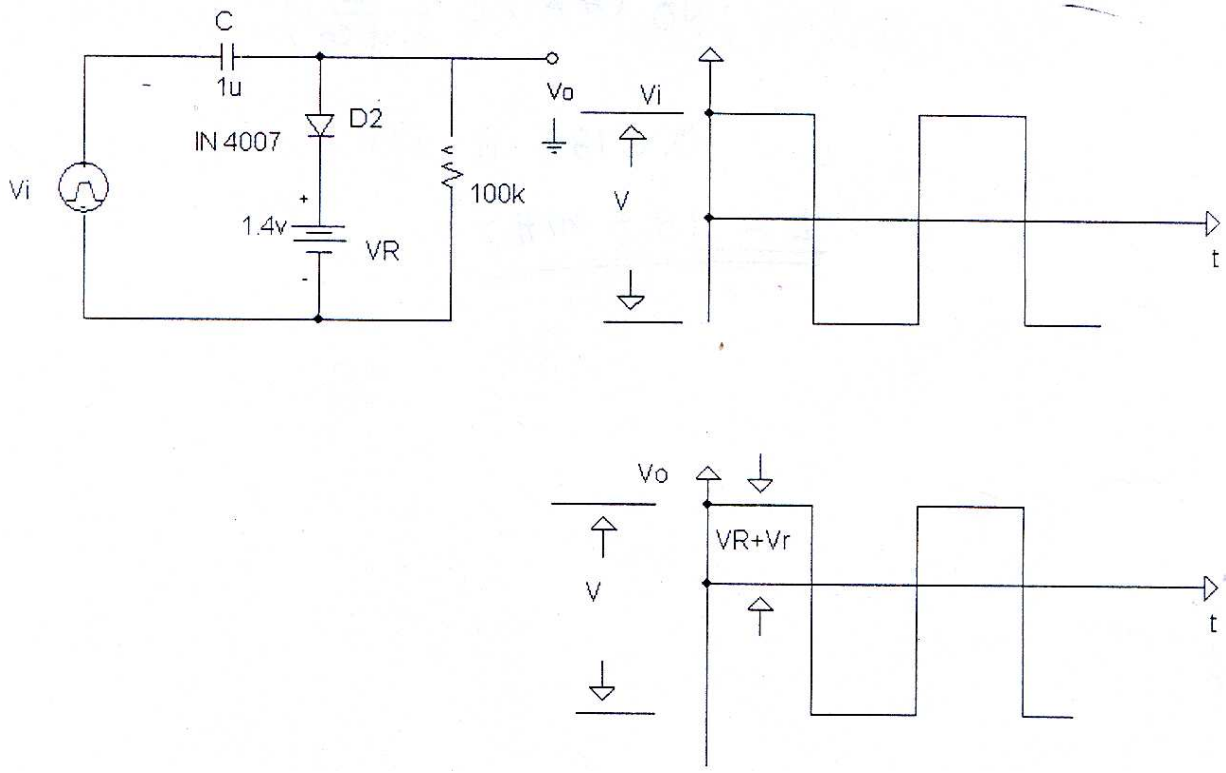


Circuit Diagram:-

a) Positive peak clamped at Vr level :-



b) Positive peak clamped at +ve Reference :-



Experiment No: **DATE: __/__/____**

CLAMPING CIRCUITS

AIM: - To design a Clamping circuit for the given specifications and hence to plot its output.

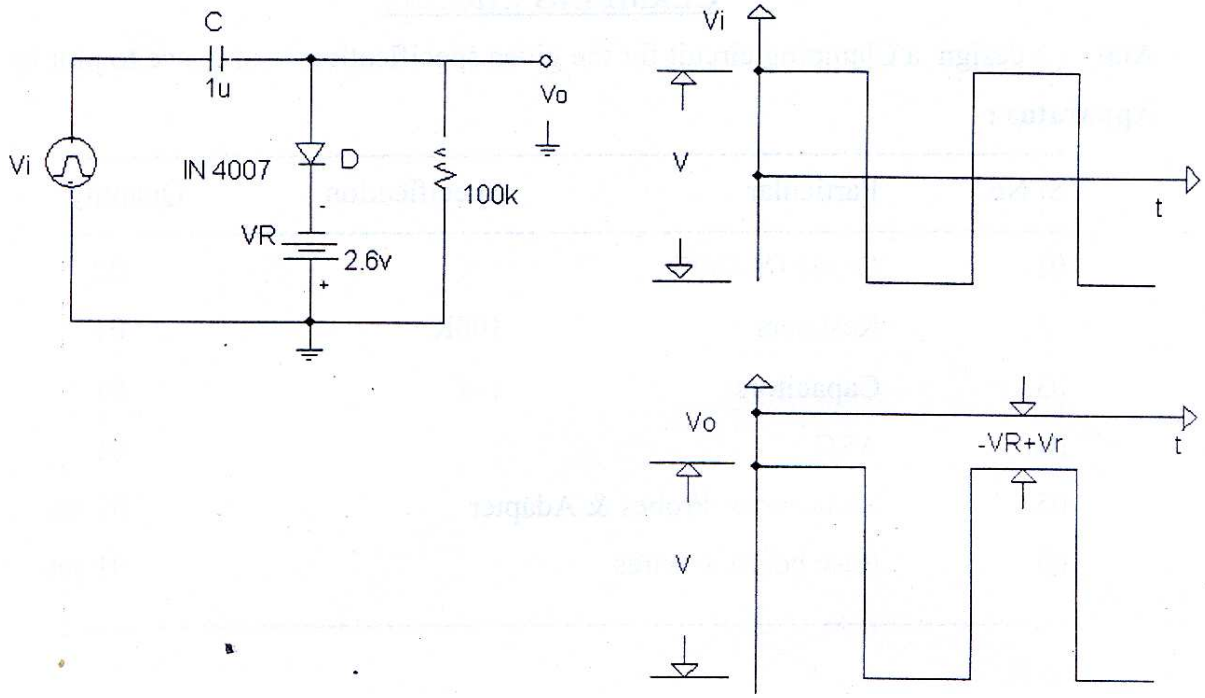
APPARATUS REQUIRED:-

Diode-IN 4007, capacitors, resistors, power supply, CRO, function generator, multimeter, etc.

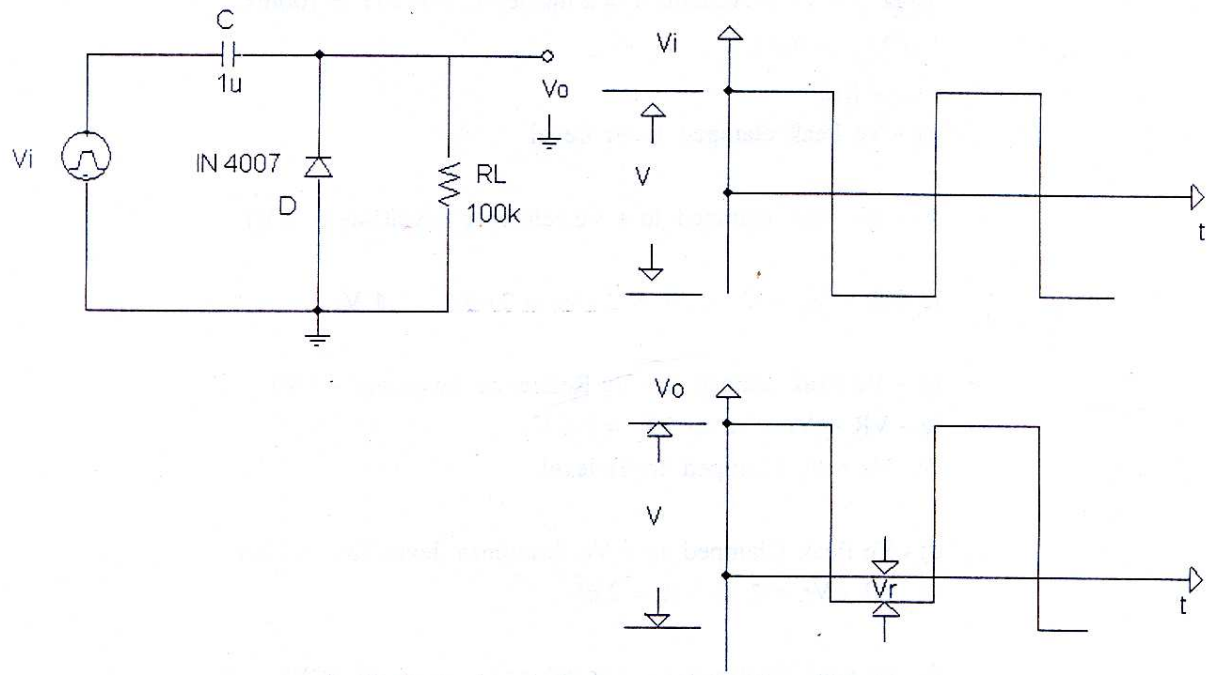
PROCEDURE: -

1. Connections are made as shown in the circuit diagram.
2. A square wave input Vi is applied
3. Output waveform Vo is observed on the CRO. Keeping the AC/DC switch of the CRO in DC Position.
4. Clamped voltage is measured and verified with the designed values.

c) Positive peak clamped at –ve reference level :-



d) Negative peak clamped to Vr level :-



DESIGN :-

$R_L C >> T$ => Assume T = 2 ms, let $R_L C = 50T = 100ms$

Let $R_L = 100K\Omega$

$\therefore C = 1\mu f$

a) Positive peak clamped to Vr level

b) Positive clamped to +ve reference level (say +2v)

ie., VR + Vr = 2 => VR = 2-Vr = 2 – 0.6 = 1.4v

c) Positive peak clamped to –ve reference level (say -2v)

ie., -VR + Vr = -2 => VR = 2.6v

d) Negative peak clamped to Vr level

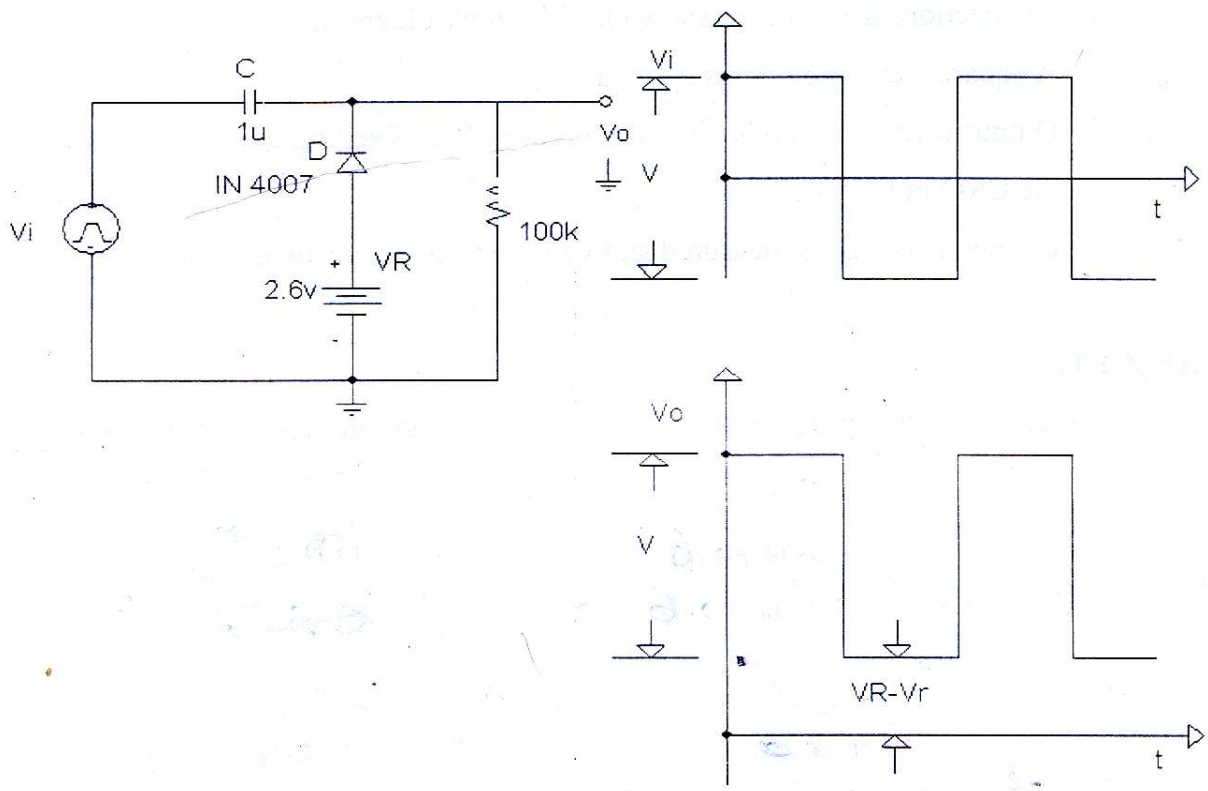
e) Negative peak clamped to +ve reference level (say +2v)

ie., VR – Vr = 2 => VR = 2.6v

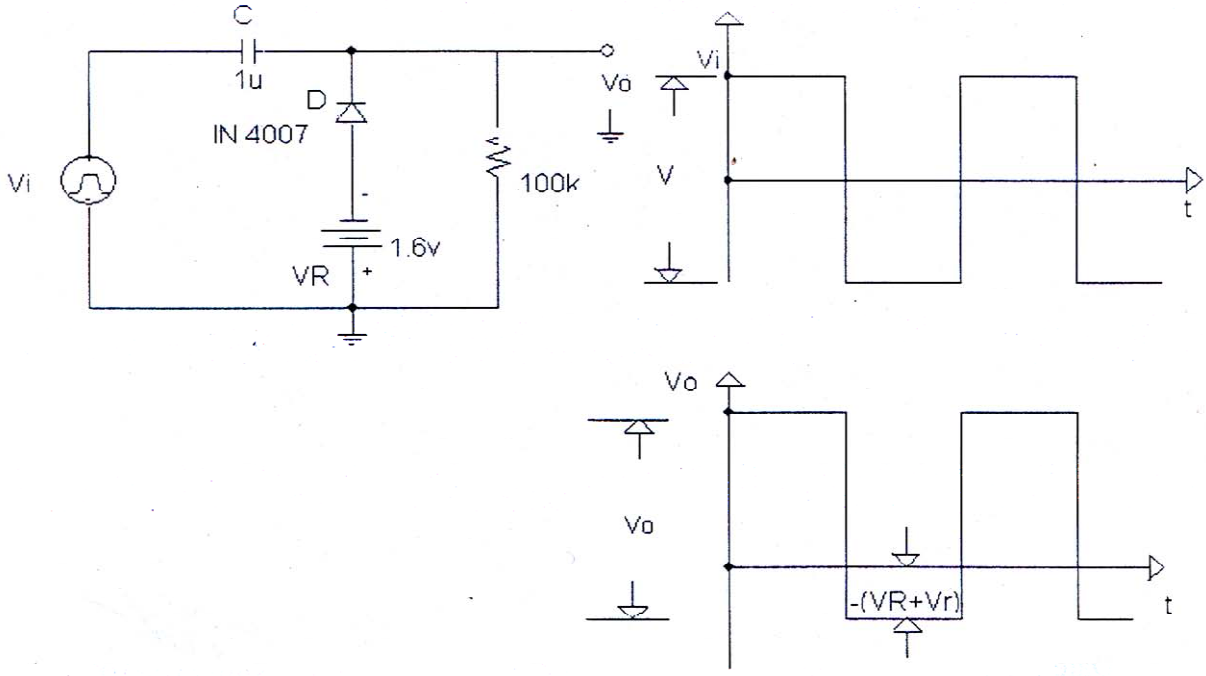
f) Negative peak clamped to –ve reference level (say -2v)

ie., (VR+Vr) = -2 => VR = 1.6v

e) Negative peak clamped at +ve reference level :-



f) Negative peak clamped at –ve reference level :-

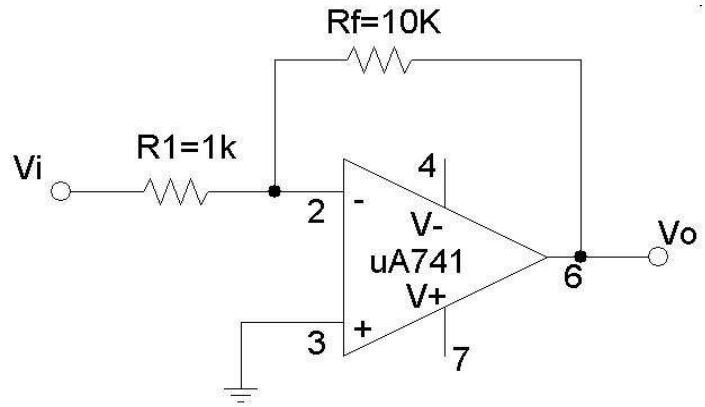


RESULT :-

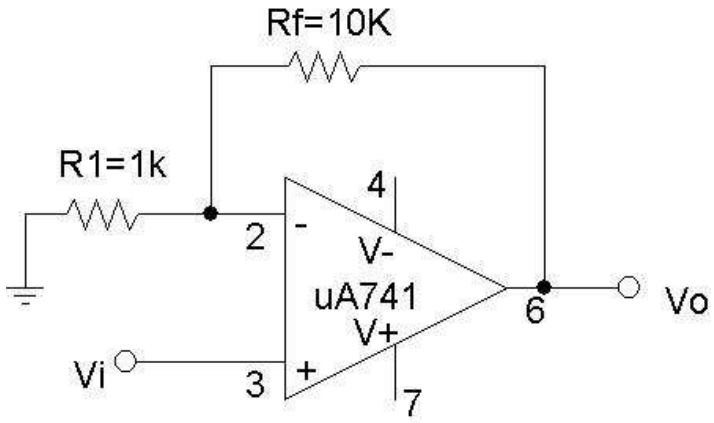
Circuit	Clamping level (Designed)	Clamping level (Observed)
a)		
b)		
c)		
d)		
e)		
f)		

Circuit Diagram:-

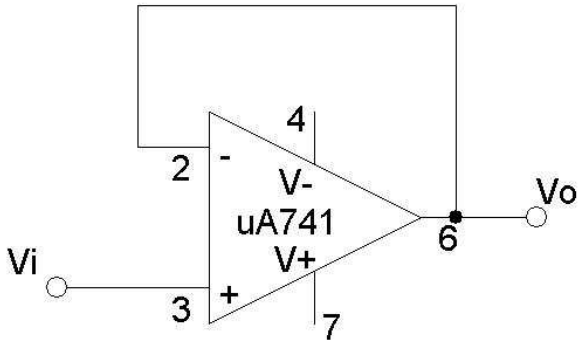
INVERTING AMPLIFIER:-



NONINVERTING AMPLIFIER:-



VOLTAGE FOLLOWER:-



Experiment No: **DATE: __/__/____**

LINEAR APPLICATIONS OF OP-AMP

AIM:- To design and test Operational amplifier applications: (1)Inverting Amplifier, (2) Non-Inverting Amplifier, (3) Summer, (4) Voltage Follower, (5) Integrator and Differentiator.

APPARATUS REQUIRED:-

Op-Amp – μA 741, capacitors, resistor, Dual power supply, Regulated power supply, CRO, function generator, multimeter, etc.

PROCEDURE: -

1. Connect the circuit as per the circuit diagram.
2. Give the input signal as specified
3. Switch on the dual power supply.
4. Note down the outputs from the CRO.
5. Draw the necessary waveforms on the graph sheet.
6. Repeat the procedure for all circuits.

DESIGN:-

a) Inverting Amplifier: Let Av = 10 = $\frac{-Rf}{Ri}$

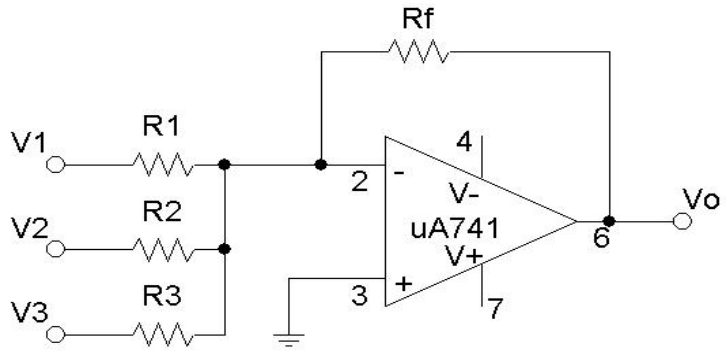
Assume Ri = 1kΩ ∴ Rf = 10 KΩ, Ri = 10KΩ

b) Non Inverting Amplifier Let Av = 11 =1 + $\frac{Rf}{Ri}$

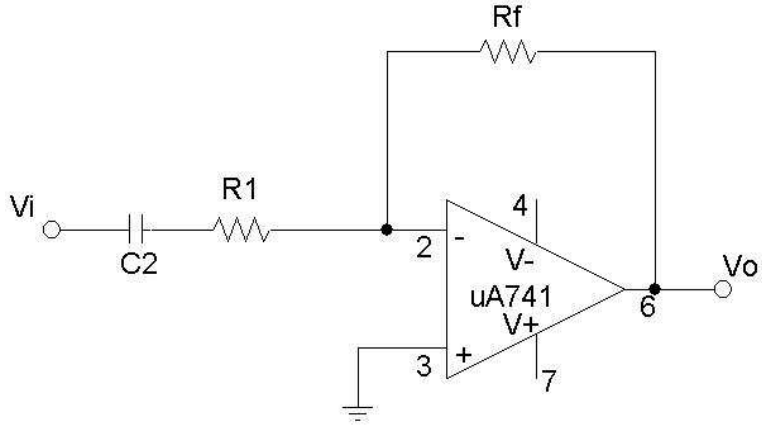
Assume Ri =1kΩ ∴ Rf = (11-1) × $Ri = 10k\Omega$

c) Voltage follower Av =unity.

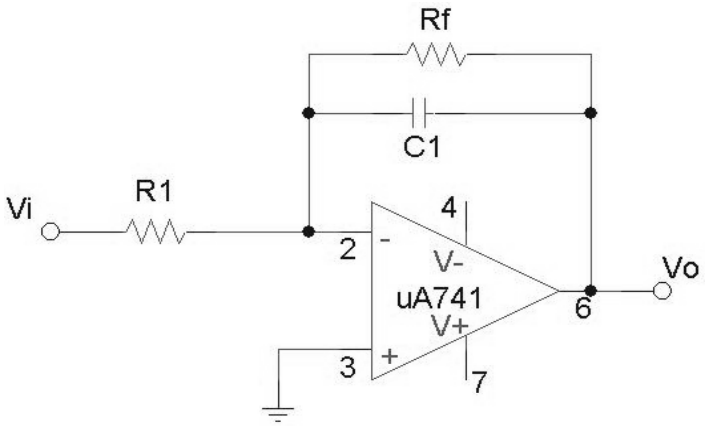
SUMMER:-



DIFFERENTIATOR:-



INTEGRATOR:-



DESIGN:-

a) Integrator

RC>>T

Let T=1msec and RC = 100 T = 100 msec

Assume R = 100 KΩ $\therefore$ C = 1μμ

Assume Rf = 10 KΩ

b) Differentiator:-

RC<<T

Let T =1msec and Rc =0.01μf

Assume R =1KΩ

c) Summer:-

Let Y=2V1+V2+3V3= $\frac{Rf}{R1}V1+\frac{Rf}{R2}V2+\frac{Rf}{R3}V3$

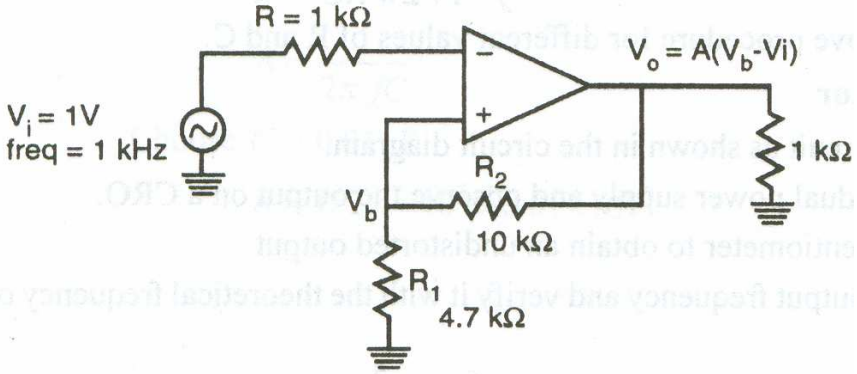
i.e, $\therefore \frac{Rf}{R1}=2,\frac{Rf}{R2}=1 and \frac{Rf}{R3}V3$

Assume Fr = 10kΩ $\therefore$ R1=5KΩ, R2=10kΩ and R3=3.33kΩ

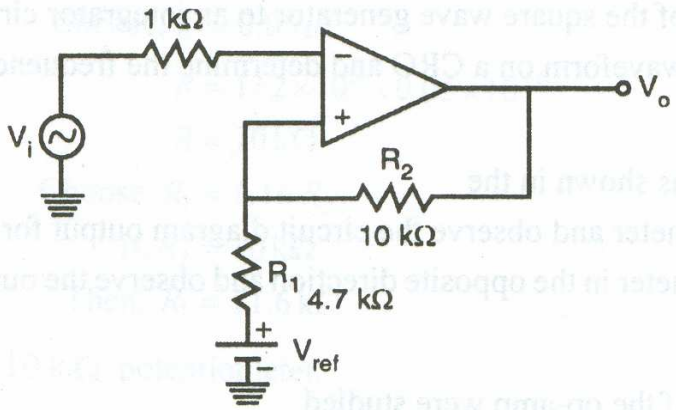
Assume R = 10kΩ

Circuit Diagram:-

Schmitt trigger with zero-reference

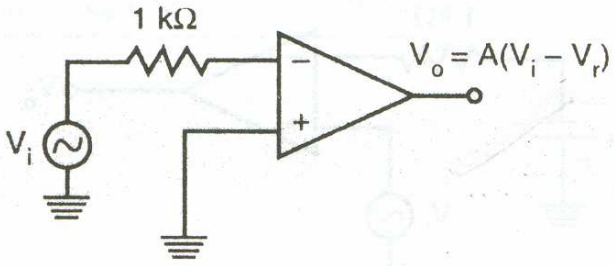


Schmitt trigger with positive reference



Comparator: Zero Crossing Detector

$$V_0 = +V_{sat}, \text{ when } V_i < 0$$
$$V_0 = -V_{sat}, \text{ when } V_i > 0$$



Experiment No: **DATE: __/__/____**

SCHMITT TRIGGER

AIM:- To design and test USING Operational amplifiers for the performance of: (1)Zero Crossing Detector, (2) Schmitt Trigger for different hysterisis values.

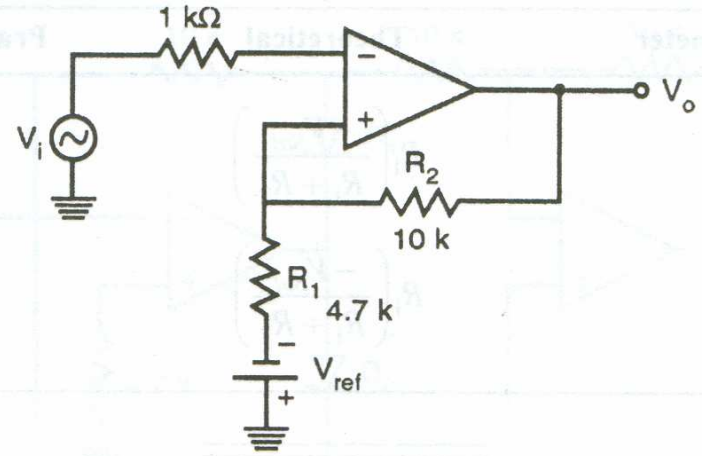
APPARATUS REQUIRED:-

Op-Amp – μA 741, capacitors, resistor, Dual power supply, Regulated power supply, CRO, function generator, multimeter, etc.

PROCEDURE: -

1. Connect the circuit as per the circuit diagram.
2. For a zero crossing detector, connect the non-inverting terminal to ground.
3. Switch on the dual power supply.
4. Observe the output waveform on the CRO
5. Draw the output and input waveforms.
6. For Schmitt Trigger set input signal (say 1V, 1 KHz) using signal generator.
7. Observe the input and output waveforms on the CRO.
8. Plot the graphs: V_i vs Time, V_O vs Time.

Schmitt trigger with negative reference

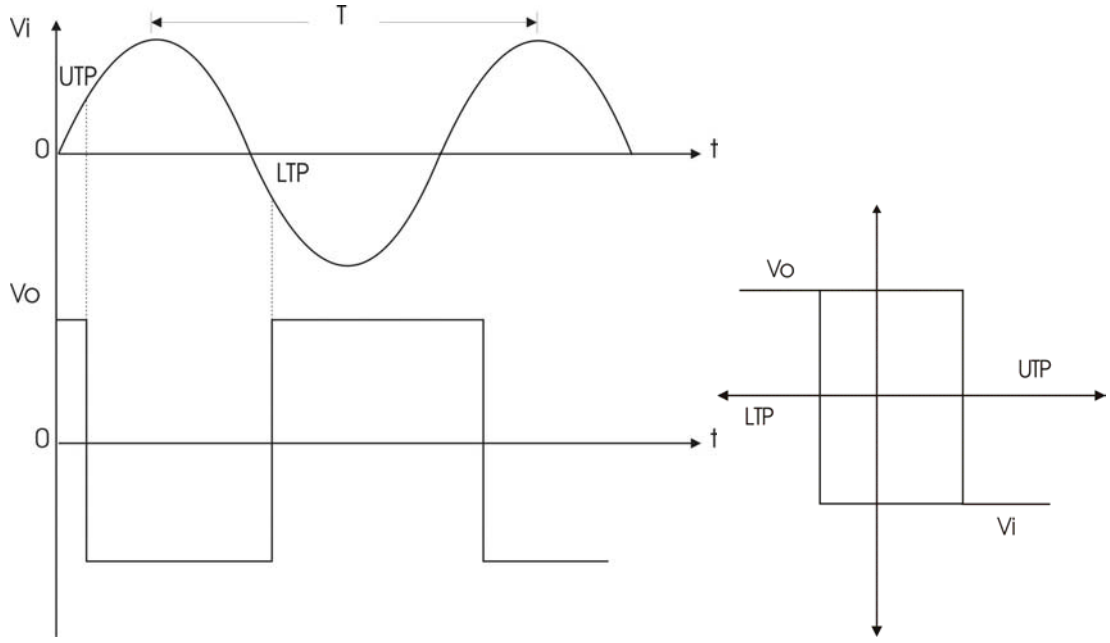


Design

Given, $V_R = 0$ and $\pm V_{sat} = \pm 12$ V.

Assume, $V_{b1} = V_{b2}$

WAVE FORMS:-



DESIGN:-

Let UTP = 6V = $\Rightarrow \frac{VRRI}{R1+R2} + \frac{VsatR2}{R1+R2}$

LTP = - 2V = $\Rightarrow \frac{VRRI}{R1+R2} + \frac{VsatR2}{R1+R2}$

Assume V_{sat} = 12V

UTP + LTP =4 = $\frac{2VRRI}{R1+R2} \Rightarrow VR = \frac{2(R1+R2)}{R1} = 2(1+\frac{R2}{R1})$

UTP - LTP =8 = $\frac{2VsatR2}{R1+R2} \Rightarrow VR = \frac{R1}{R2} = 2$

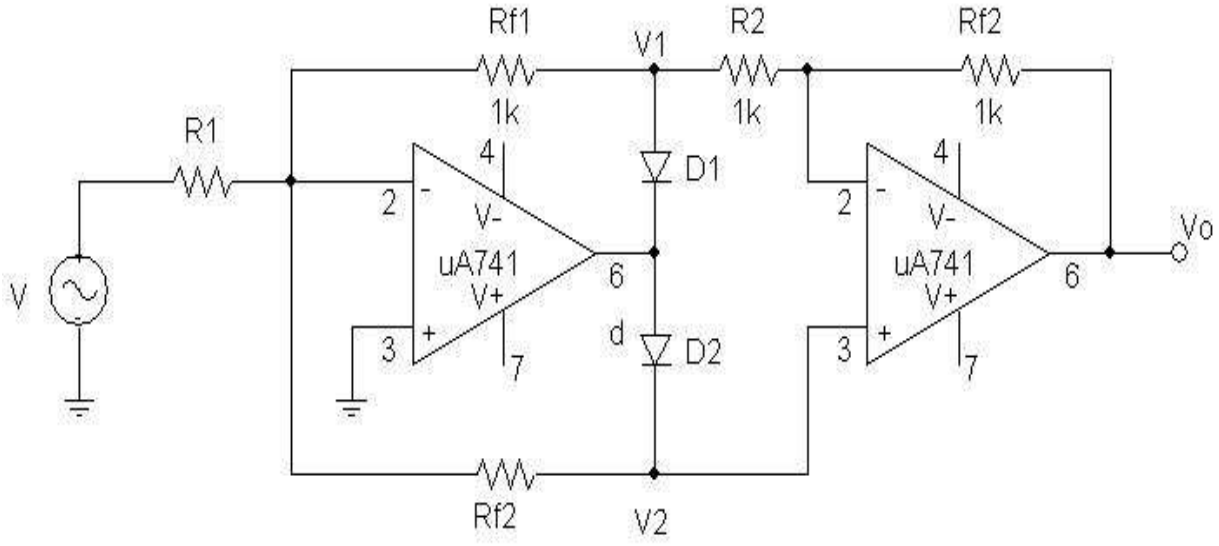
$\therefore$ VR = 3V, Assume R2 = 1 K Ω $\Rightarrow$ R1 = 2 K Ω

III^{Iy} design for UTP = + 4, +8, +2 and -2.

LTP = - 4, + 2, - 4 and = 4

RESULT: -UTP and LTP is measured and compared with the designed value.

FULL WAVE PRECISION RECTIFIER:-



DESIGN:-

(i) Given $A = \frac{5}{0.5} = 10 = \frac{Rf}{Ri}$

Assume $Ri = 1k\Omega, \therefore Rf = 10K\Omega$

Choose $R = 10K\Omega$

$Rf' = Rf = 10K\Omega$

(ii) Given $A1 = \frac{5}{0.5} = 10 = \frac{Rf}{Ri}$ **and** $A2 = \frac{3}{0.5} = 6 = 3\frac{Rf}{Ri}\left(\frac{Rf'}{2R + Rf'}\right)$

Assume $Ri = 1K\Omega$

$Rf = 10K\Omega$ **and** $Rf' = 5K\Omega$

Experiment No: **DATE: __/__/____**

FULL WAVE PRECISION RECTIFIER

AIM: - To test for the performance of Full wave Precision Rectifier using Operational Amplifier.

APPARATUS REQUIRED:-

Op-Amp – μA 741, capacitors, resistor, Dual power supply, Regulated power supply, CRO, function generator, multimeter, etc.

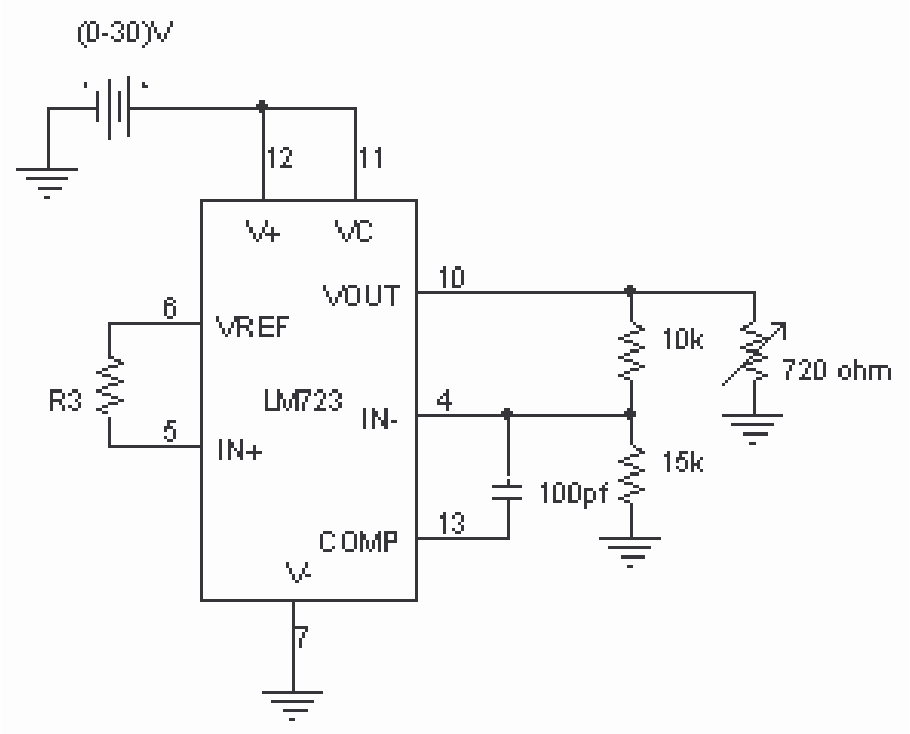
PROCEDURE: -

1. Connect the circuit as per the circuit diagram.
2. Give a sinusoidal input of VPP, 1 KHz from a signal generator.
3. Switch on the power supply and note down the output from CRO.
4. Without Connecting Rf 2, the wave form of the half wave rectifier is produced.
5. At some value of Rf 2 the wave form of a full wave rectifier is obtained.
6. Repeat the above procedure by reversing the diodes.

RESULT:-

The operation of the precision rectifier is studied using μA 741.

CIRCUIT DIAGRAM: - (HIGH VOLTAGE)



DESIGN:-

Given $V_O = 12v$

$$V_O = 7.15\left[1+\frac{R_1}{R_2}\right]$$

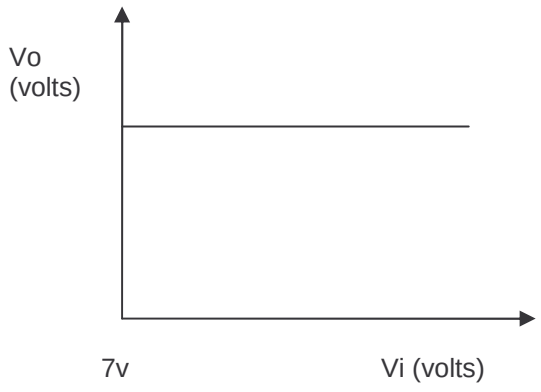
$$12 = 7.15\left[1+\frac{R_1}{R_2}\right]$$

Assume $R_1 = 10K\Omega$

$\therefore R_2 = 17.7K\Omega$ [use $15K\Omega$]

Assume $R_L = 720\Omega$ & $C = 100pf$

CHARACTERISTIC CURVE: -



OBSERVATION:-

Vi (volts)	Vo (volts)

Experiment No: **DATE: __/__/____**

VOLTAGE REGULATOR USING IC 723

AIM: - To design and test the IC 723 voltage regulator.

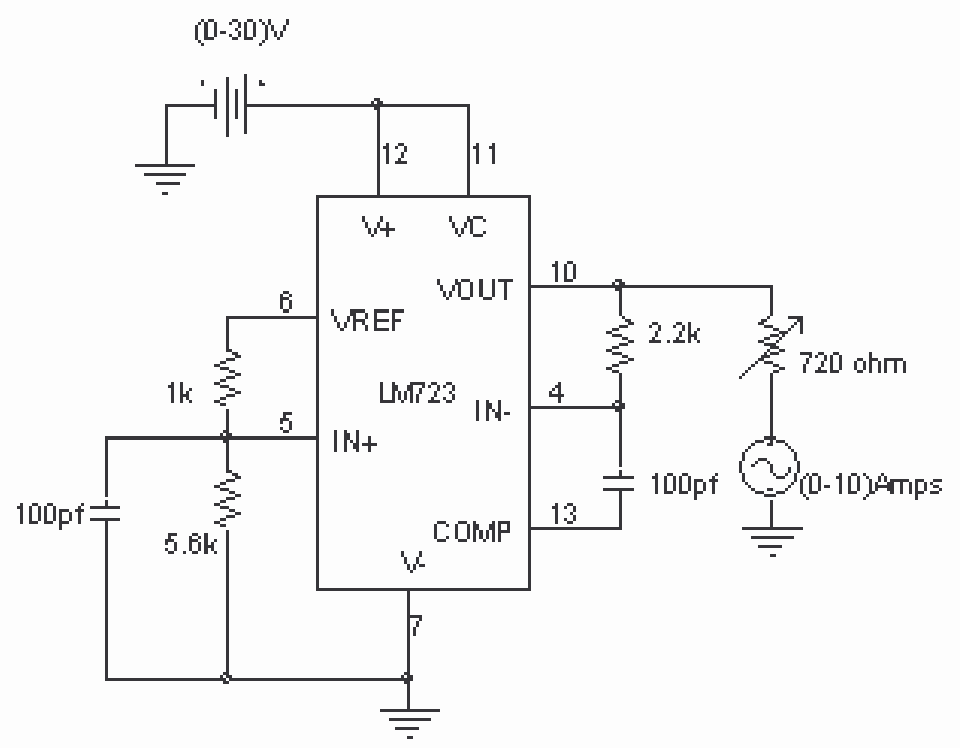
APPARATUS REQUIRED:-

IC 723, capacitors, resistor, power supply, CRO, function generator, multimeter, etc.

PROCEDURE: -

1. Connect the circuit as per the circuit diagram.
2. Switch on the power supply and note down the output from CRO.
3. Vary the input voltage from 7V, note down corresponding output voltage.
4. Draw the regulation charectistics.

CIRCUIT DIAGRAM: - (LOW VOLTAGE)



DESIGN:-

For LM723 $V_{ref} = 7.15V$

$$V_O = 7.15\left[\frac{R_2}{R_1 + 2}\right]$$

Let the devider current I_O through the resistor R_1 & R_2 is 1mA. Since error amplifier draws very little current, we will neglect its input bias current.

$$\text{Hence } R_1 = \frac{V_{ref} - V_O}{I_D} = \frac{7.15 - 6}{1\times10^3} = 1.1K\Omega$$

$$R_2 = \frac{V_O}{I_D} = \frac{6}{1\times10^3} = 6K\Omega$$

$$R_3 = \frac{R_1R_2}{R_1 + R_2} = \_\_\_\_\_$$

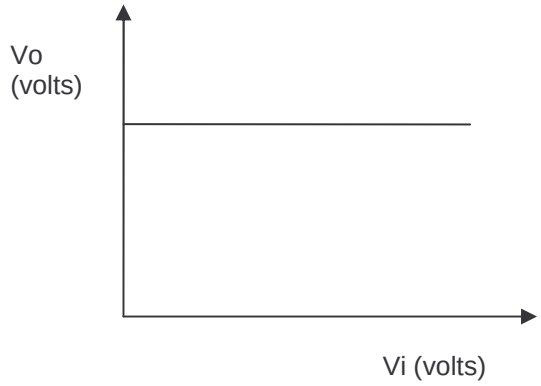
Assume $C_1 = 0.1\mu F$ & $C_2 = 100PF$

PROCEDURE:-

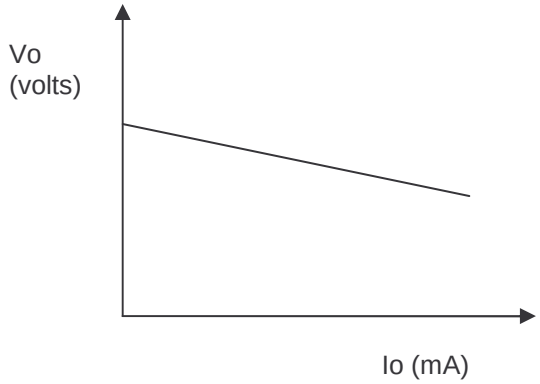
1. Connect the circuit as per the circuit diagram.
2. For line regulation vary the input voltage from 7V, note down the corresponding output voltage.
3. Draw the transfer characteristics.
4. For load regulation note down the output current.
5. Draw the transfer characteristics.

GRAPH:-

(i) Line Regulation



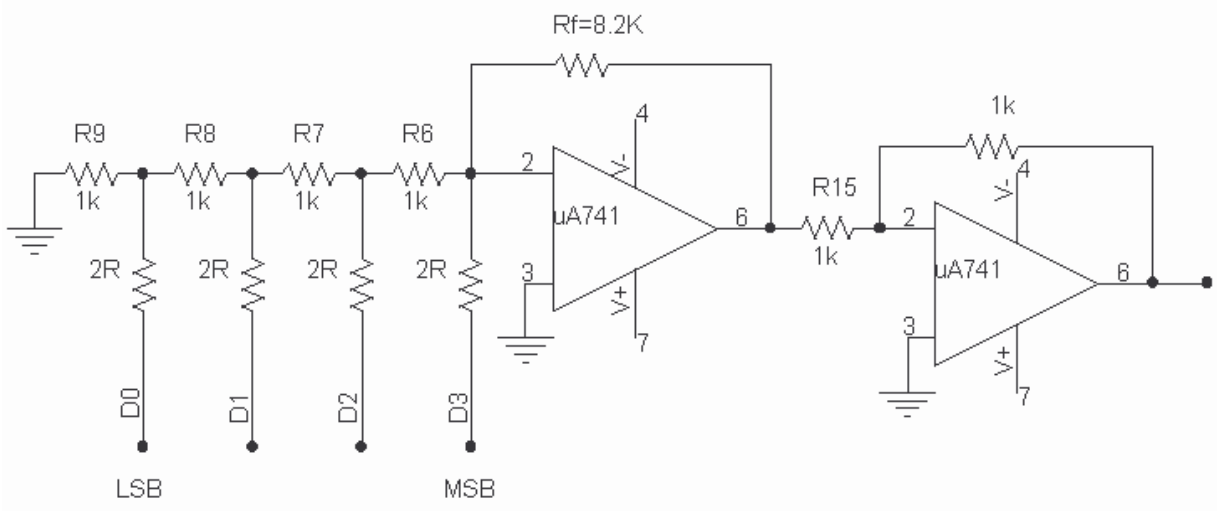
(ii) Load Regulation



OBSERVATION:-

(i) Line Regulation			**(ii) Load Regulation**	
Vi (volts)	**Vo (volts)**		**Vi (volts)**	**Vo (volts)**

CIRCUIT DIAGRAM: -



$$V_0 = -R_f\left[\frac{b_3}{2R} + \frac{b_2}{4R} + \frac{b_1}{8R} + \frac{b_0}{16R}\right] \times V_{ref}$$

Note: -

1. b_3, b_2, b_1 and b_0 are binary input.
2. V_{ref} = 5V.
3. If b is the decimal value of the binary input b_3, b_2, b_1, b_0, then $V_0 = \frac{-V_{ref}}{8} \times b$
4. Vo is the analog output
5. Binary inputs can either take the value 0 or 1
6. Binary input b_i can be made 0 by connecting the input to the ground. It can be made 1 by connecting to +5V

Experiment No: **DATE: __/__/____**

VOLTAGE REGULATOR USING IC 723

AIM: - To design 4 bit R-2R ladder DAC using op-amp.

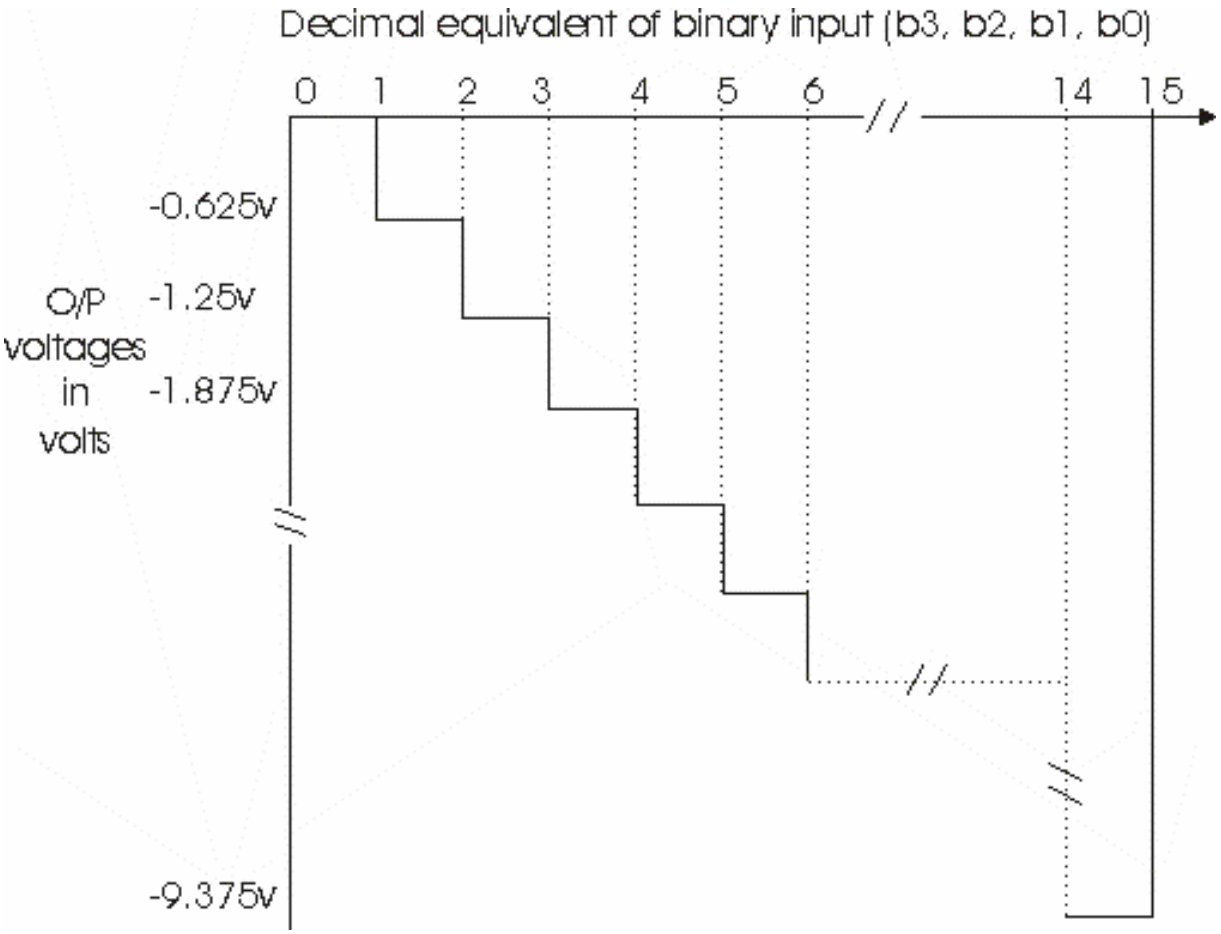
APPARATUS REQUIRED:-

IC 723, resistor, power supply, CRO, multimeter, etc.

PROCEDURE: -

1. Connect the circuit as per the circuit diagram.
2. The IC is given proper bias of '+12V' and '-12V' to 'Vcc' and 'Vee' respectively.
3. According to the binary values of b_3, b_2, b_1 and b_0, b_3, b_2, b_1 and b_0 are connected to '+5V' or 'Ground' respectively.
4. The o/p voltage is tabulated for different binary inputs and is compared with the theoretical values.

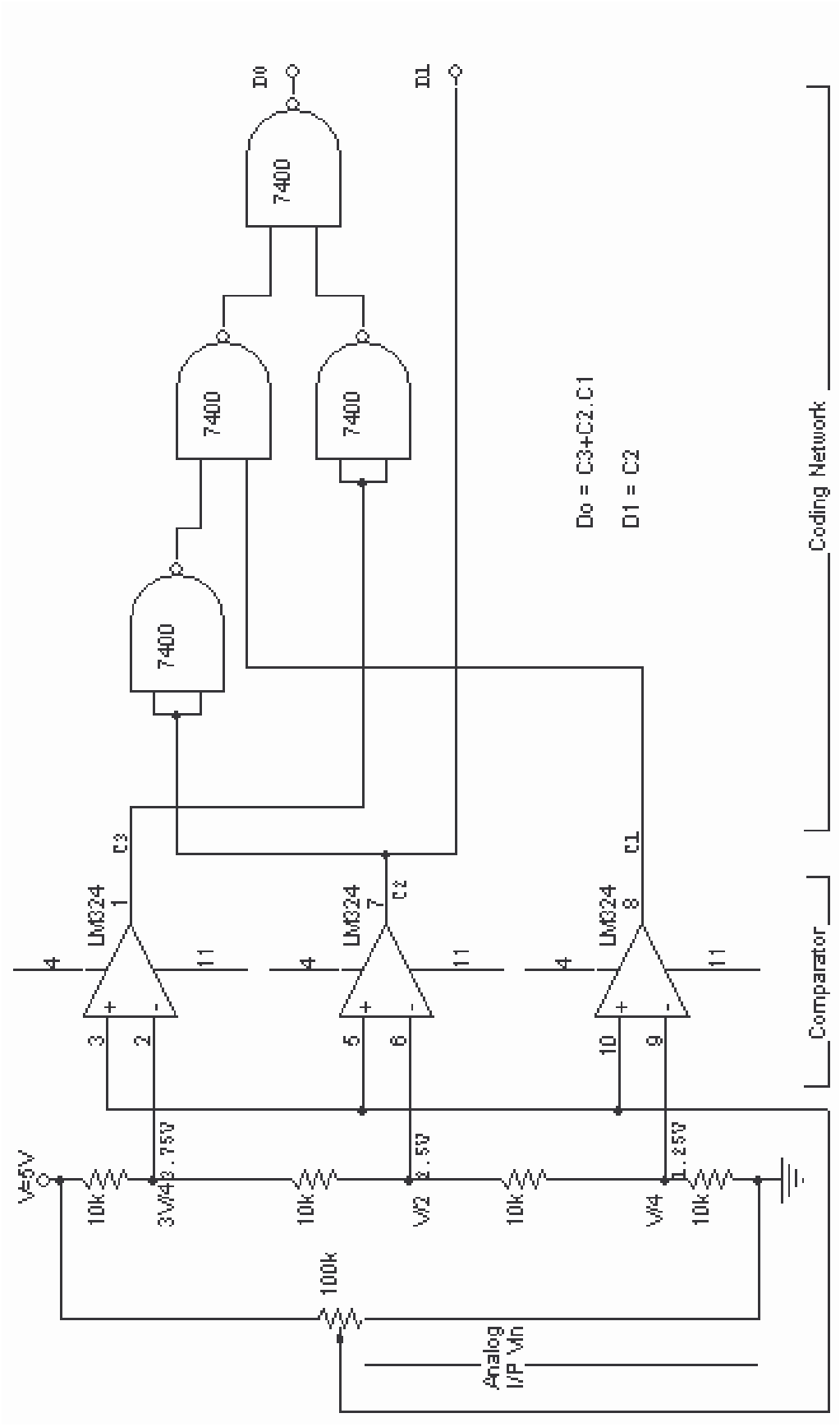
O/P vs I/P


Decimal equivalent of binary input (b3, b2, b1, b0)
0
1
2
3
4
5
6
14
15
-0.625v
-1.25v
-1.875v
-9.375v
O/P voltages in volts

Tabular Column:-

Inputs				Output (volts)	
b_3	b_2,	b_1	b_0	Practical	Theoretical
0	0	0	0		
0	0	0	1		
0	0	1	0		
0	0	1	1		
0	1	0	0		
0	1	0	1		
0	1	1	0		
0	1	1	1		
1	0	0	0		
1	0	0	1		
1	0	1	0		
1	0	1	1		
1	1	0	0		
1	1	0	1		
1	1	1	0		
1	1	1	1		

CIRCUIT DIAGRAM: - (2 BIT Flash type ADC)



Experiment No: **DATE: __/__/____**

ANALOG TO DIGITAL CONVERTOR

AIM: - To rig up circuit to convert an analog voltage to its digital equivalent

APPARATUS REQUIRED:-

IC LM 324, IC 7400, resistor, power supply, multimeter, etc.

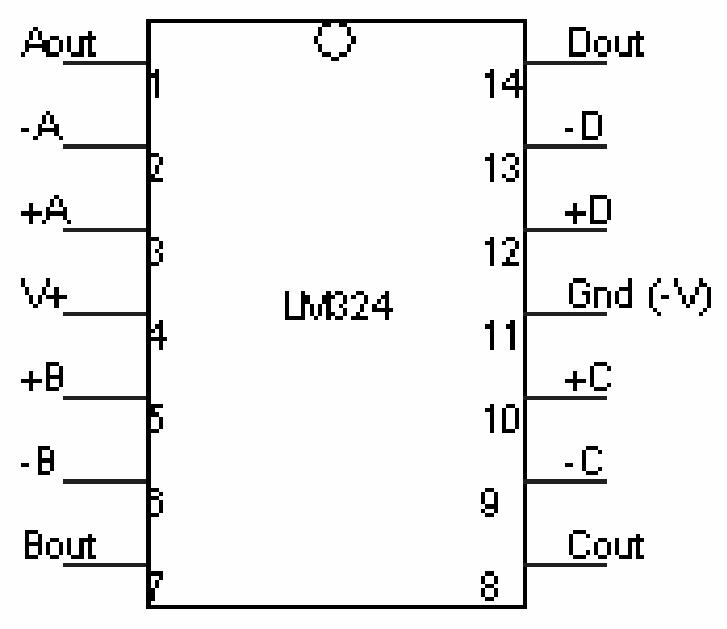
PROCEDURE: -

1. Connect the circuit as per the circuit diagram.
2. Verify the digital O/P for different analog voltages.

Note:- (1). Connect V+ (pin 4) terminal of the OPAMP to +5V
(2). Connect V- (pin 11) terminal of the OPAMP to ground

Design: Number of comparators required = 2n-1
Where n = desired number of bits
C1, C2 & C3 = Comparator o/p
D0 & D1 = Encoder (Coding network) O/P

PIN DIAGRAM:-


Aout
1
-A
2
+A
3
V+
4
+B
5
-B
6
Bout
7
LM324
14
Dout
13
-D
12
+D
11
Gnd (-V)
10
+C
9
-C
8
Cout

Tabular Column:-

Analog I/P Vin	C3	C2	C1	D1	D0
0 to v/4	0	0	0	0	0
V/4 to V/2	0	0	1	0	1
V/2 to 3V/4	0	1	1	1	0
3V/4 to V	1	1	1	1	1